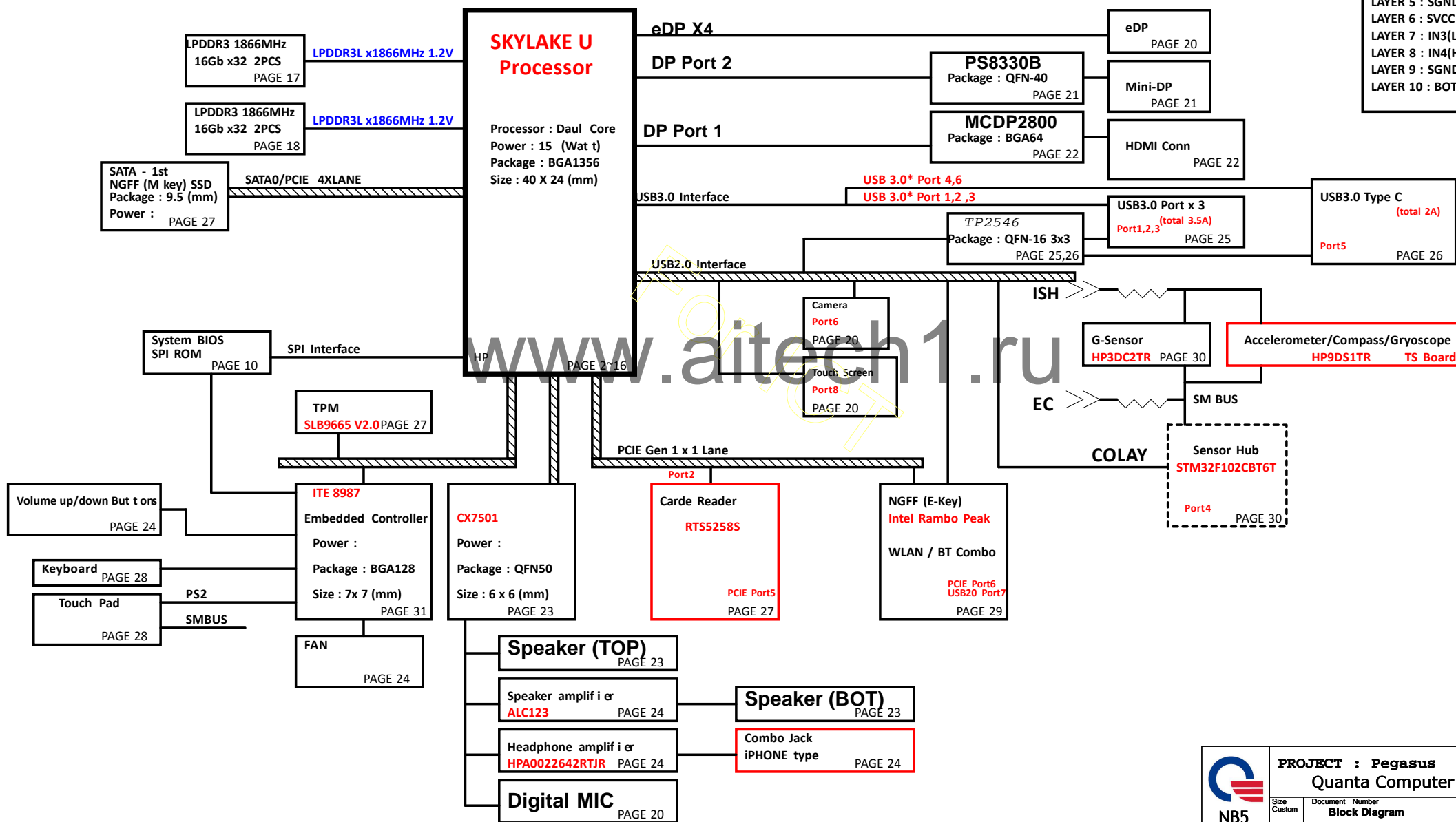


# Pegasus Intel SKYLAKE ULT Plat f or mB ock D a g r a m

PCB 10L STACK UP

LAYER 1 : TOP  
 LAYER 2 : SGND  
 LAYER 3 : IN1(High)  
 LAYER 4 : IN2(High)  
 LAYER 5 : SGND  
 LAYER 6 : SVCC  
 LAYER 7 : IN3(Low)  
 LAYER 8 : IN4(High)  
 LAYER 9 : SGND  
 LAYER 10 : BOT



## HDMI

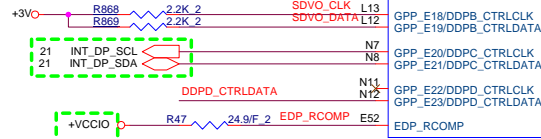
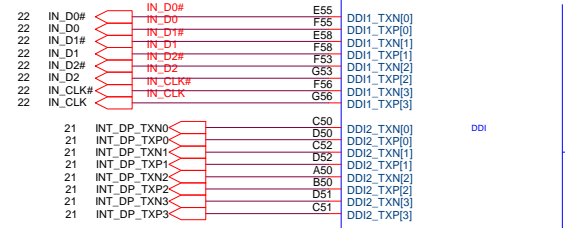
+3V 4,10,11,12,13,14,15,16,20,21,22,23,24,27,28,30,31,38,39  
+1.0V 4,6,16,31,37  
+VCCSTPLL 4,5,6,9,37,39  
+VCCIO 6,16,37

INT\_DP\_SCL R245 2.2K 2  
INT\_DP\_SDA R246 2.2K 2

DDPB\_CTRLDATA/ GPP\_E19  
Display Port B Detected  
This signal has a weak internal pull-down.  
0 = Port B is not detected.  
1 = Port B is detected.

This signal has a weak internal pull-down.  
0 = Port C and D is not detected.  
1 = Port C and D is detected.

DDPD\_CTRLDATA R51 10K 2



EDP\_CMPIO and ICMPIO signals should be shorted near balls and routed with typical impedance <25 mohms

## Need apply PN

DDI

EDP

DISPLAY SIDE BANDS

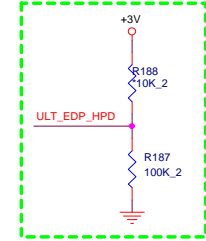
1 OF 20

?

Reserve EDP\_HPD opposites circuit!

## HDMI 2.0

## Mini-DP



## Need apply PN

SKL\_ULT ?

JTAG

CPU\_MGC

PROC\_TCK

PROC\_TDI

PROC\_TDO

PROC\_TMS

PROC\_TRST#

JTAGX

JTAG\_TCK\_PCH

JTAG\_TDI\_PCH

JTAG\_TDO\_PCH

JTAG\_TMS\_PCH

JTAG\_TRST#\_CPU

JTAGX\_PCH

XDP\_TCK0

XDP\_TDI\_CPU

XDP\_TDO\_CPU

XDP\_TMS\_CPU

XDP\_TRST#\_CPU

JTAG\_TCK\_PCH

JTAG\_TDI\_PCH

JTAG\_TDO\_PCH

JTAG\_TMS\_PCH

JTAG\_TRST#\_CPU

JTAGX\_PCH

XDP\_TCK0

XDP\_TDI\_CPU

XDP\_TDO\_CPU

XDP\_TMS\_CPU

XDP\_TRST#\_CPU

JTAG\_TCK\_PCH

JTAG\_TDI\_PCH

JTAG\_TDO\_PCH

JTAG\_TMS\_PCH

JTAG\_TRST#\_CPU

JTAGX\_PCH

XDP\_TCK0

XDP\_TDI\_CPU

XDP\_TDO\_CPU

XDP\_TMS\_CPU

XDP\_TRST#\_CPU

JTAG\_TCK\_PCH

JTAG\_TDI\_PCH

JTAG\_TDO\_PCH

JTAG\_TMS\_PCH

JTAG\_TRST#\_CPU

JTAGX\_PCH

XDP\_TCK0

XDP\_TDI\_CPU

XDP\_TDO\_CPU

XDP\_TMS\_CPU

XDP\_TRST#\_CPU

JTAG\_TCK\_PCH

JTAG\_TDI\_PCH

JTAG\_TDO\_PCH

JTAG\_TMS\_PCH

JTAG\_TRST#\_CPU

JTAGX\_PCH

XDP\_TCK0

XDP\_TDI\_CPU

XDP\_TDO\_CPU

XDP\_TMS\_CPU

XDP\_TRST#\_CPU

JTAG\_TCK\_PCH

JTAG\_TDI\_PCH

JTAG\_TDO\_PCH

JTAG\_TMS\_PCH

JTAG\_TRST#\_CPU

JTAGX\_PCH

XDP\_TCK0

XDP\_TDI\_CPU

XDP\_TDO\_CPU

XDP\_TMS\_CPU

XDP\_TRST#\_CPU

JTAG\_TCK\_PCH

JTAG\_TDI\_PCH

JTAG\_TDO\_PCH

JTAG\_TMS\_PCH

JTAG\_TRST#\_CPU

JTAGX\_PCH

XDP\_TCK0

XDP\_TDI\_CPU

XDP\_TDO\_CPU

XDP\_TMS\_CPU

XDP\_TRST#\_CPU

JTAG\_TCK\_PCH

JTAG\_TDI\_PCH

JTAG\_TDO\_PCH

JTAG\_TMS\_PCH

JTAG\_TRST#\_CPU

JTAGX\_PCH

XDP\_TCK0

XDP\_TDI\_CPU

XDP\_TDO\_CPU

XDP\_TMS\_CPU

XDP\_TRST#\_CPU

JTAG\_TCK\_PCH

JTAG\_TDI\_PCH

JTAG\_TDO\_PCH

JTAG\_TMS\_PCH

JTAG\_TRST#\_CPU

JTAGX\_PCH

XDP\_TCK0

XDP\_TDI\_CPU

XDP\_TDO\_CPU

XDP\_TMS\_CPU

XDP\_TRST#\_CPU

JTAG\_TCK\_PCH

JTAG\_TDI\_PCH

JTAG\_TDO\_PCH

JTAG\_TMS\_PCH

JTAG\_TRST#\_CPU

JTAGX\_PCH

XDP\_TCK0

XDP\_TDI\_CPU

XDP\_TDO\_CPU

XDP\_TMS\_CPU

XDP\_TRST#\_CPU

JTAG\_TCK\_PCH

JTAG\_TDI\_PCH

JTAG\_TDO\_PCH

JTAG\_TMS\_PCH

JTAG\_TRST#\_CPU

JTAGX\_PCH

XDP\_TCK0

XDP\_TDI\_CPU

XDP\_TDO\_CPU

XDP\_TMS\_CPU

XDP\_TRST#\_CPU

JTAG\_TCK\_PCH

JTAG\_TDI\_PCH

JTAG\_TDO\_PCH

JTAG\_TMS\_PCH

JTAG\_TRST#\_CPU

JTAGX\_PCH

XDP\_TCK0

XDP\_TDI\_CPU

XDP\_TDO\_CPU

XDP\_TMS\_CPU

XDP\_TRST#\_CPU

JTAG\_TCK\_PCH

JTAG\_TDI\_PCH

JTAG\_TDO\_PCH

JTAG\_TMS\_PCH

JTAG\_TRST#\_CPU

JTAGX\_PCH

XDP\_TCK0

XDP\_TDI\_CPU

XDP\_TDO\_CPU

XDP\_TMS\_CPU

XDP\_TRST#\_CPU

JTAG\_TCK\_PCH

JTAG\_TDI\_PCH

JTAG\_TDO\_PCH

JTAG\_TMS\_PCH

JTAG\_TRST#\_CPU

JTAGX\_PCH

XDP\_TCK0

XDP\_TDI\_CPU

XDP\_TDO\_CPU

XDP\_TMS\_CPU

XDP\_TRST#\_CPU

JTAG\_TCK\_PCH

JTAG\_TDI\_PCH

JTAG\_TDO\_PCH

JTAG\_TMS\_PCH

JTAG\_TRST#\_CPU

JTAGX\_PCH

XDP\_TCK0

XDP\_TDI\_CPU

XDP\_TDO\_CPU

XDP\_TMS\_CPU

XDP\_TRST#\_CPU

JTAG\_TCK\_PCH

JTAG\_TDI\_PCH

JTAG\_TDO\_PCH

JTAG\_TMS\_PCH

JTAG\_TRST#\_CPU

JTAGX\_PCH

XDP\_TCK0

XDP\_TDI\_CPU

XDP\_TDO\_CPU

XDP\_TMS\_CPU

XDP\_TRST#\_CPU

JTAG\_TCK\_PCH

JTAG\_TDI\_PCH

JTAG\_TDO\_PCH

JTAG\_TMS\_PCH

JTAG\_TRST#\_CPU

JTAGX\_PCH

XDP\_TCK0

XDP\_TDI\_CPU

XDP\_TDO\_CPU

XDP\_TMS\_CPU

XDP\_TRST#\_CPU

JTAG\_TCK\_PCH

JTAG\_TDI\_PCH

JTAG\_TDO\_PCH

JTAG\_TMS\_PCH

JTAG\_TRST#\_CPU

JTAGX\_PCH

XDP\_TCK0

XDP\_TDI\_CPU

XDP\_TDO\_CPU

XDP\_TMS\_CPU

XDP\_TRST#\_CPU

JTAG\_TCK\_PCH

JTAG\_TDI\_PCH

JTAG\_TDO\_PCH

JTAG\_TMS\_PCH

JTAG\_TRST#\_CPU

JTAGX\_PCH

XDP\_TCK0

XDP\_TDI\_CPU

XDP\_TDO\_CPU

XDP\_TMS\_CPU

XDP\_TRST#\_CPU

JTAG\_TCK\_PCH

JTAG\_TDI\_PCH

JTAG\_TDO\_PCH

JTAG\_TMS\_PCH

JTAG\_TRST#\_CPU

JTAGX\_PCH

XDP\_TCK0

XDP\_TDI\_CPU

XDP\_TDO\_CPU

XDP\_TMS\_CPU

XDP\_TRST#\_CPU

JTAG\_TCK\_PCH

JTAG\_TDI\_PCH

JTAG\_TDO\_PCH

JTAG\_TMS\_PCH

JTAG\_TRST#\_CPU

JTAGX\_PCH

XDP\_TCK0

XDP\_TDI\_CPU

XDP\_TDO\_CPU

XDP\_TMS\_CPU

XDP\_TRST#\_CPU

JTAG\_TCK\_PCH

JTAG\_TDI\_PCH

JTAG\_TDO\_PCH

JTAG\_TMS\_PCH

JTAG\_TRST#\_CPU

JTAGX\_PCH

XDP\_TCK0

XDP\_TDI\_CPU

XDP\_TDO\_CPU

XDP\_TMS\_CPU

XDP\_TRST#\_CPU

JTAG\_TCK\_PCH

JTAG\_TDI\_PCH

JTAG\_TDO\_PCH

JTAG\_TMS\_PCH

JTAG\_TRST#\_CPU

JTAGX\_PCH

XDP\_TCK0

XDP\_TDI\_CPU

XDP\_TDO\_CPU

XDP\_TMS\_CPU

XDP\_TRST#\_CPU

JTAG\_TCK\_PCH

JTAG\_TDI\_PCH

JTAG\_TDO\_PCH

JTAG\_TMS\_PCH

JTAG\_TRST#\_CPU

JTAGX\_PCH

XDP\_TCK0

XDP\_TDI\_CPU

XDP\_TDO\_CPU

XDP\_TMS\_CPU

XDP\_TRST#\_CPU

JTAG\_TCK\_PCH

JTAG\_TDI\_PCH

JTAG\_TDO\_PCH

JTAG\_TMS\_PCH

JTAG\_TRST#\_CPU

JTAGX\_PCH

XDP\_TCK0

XDP\_TDI\_CPU

XDP\_TDO\_CPU

XDP\_TMS\_CPU

XDP\_TRST#\_CPU

JTAG\_TCK\_PCH

JTAG\_TDI\_PCH

JTAG\_TDO\_PCH

JTAG\_TMS\_PCH

JTAG\_TRST#\_CPU

JTAGX\_PCH

XDP\_TCK0

XDP\_TDI\_CPU

XDP\_TDO\_CPU

XDP\_TMS\_CPU

XDP\_TRST#\_CPU

JTAG\_TCK\_PCH

JTAG\_TDI\_PCH

JTAG\_TDO\_PCH

JTAG\_TMS\_PCH

JTAG\_TRST#\_CPU

JTAGX\_PCH

XDP\_TCK0

XDP\_TDI\_CPU

XDP\_TDO\_CPU

XDP\_TMS\_CPU

XDP\_TRST#\_CPU

JTAG\_TCK\_PCH

JTAG\_TDI\_PCH

JTAG\_TDO\_PCH

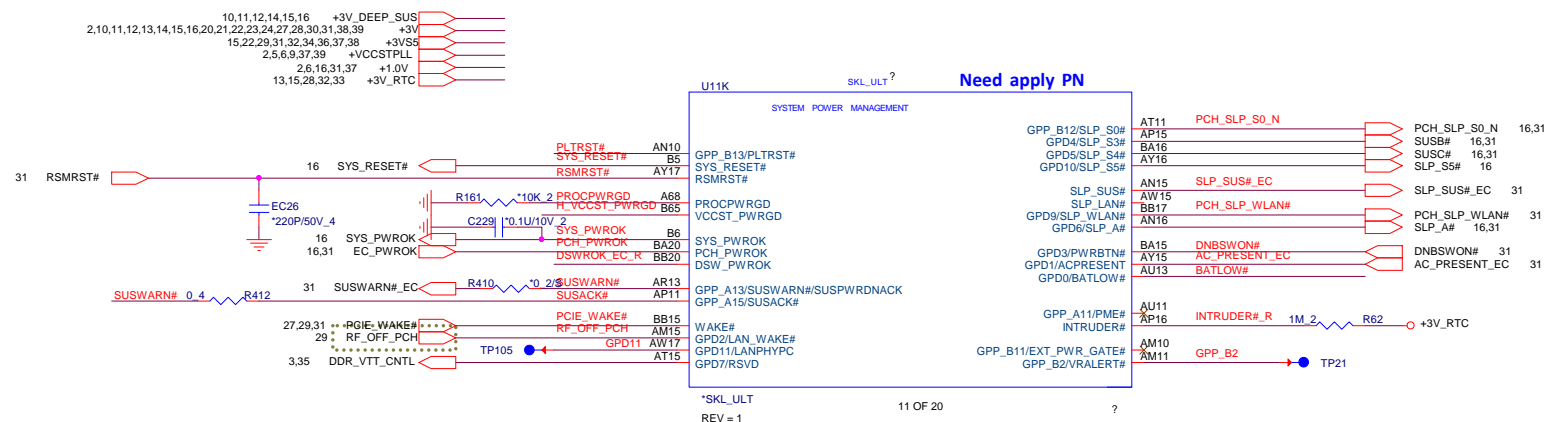
JTAG\_TMS\_PCH

JTAG\_TRST#\_CPU

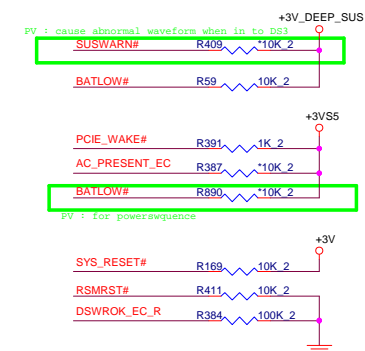
JTAGX\_PCH

XDP\_TCK0

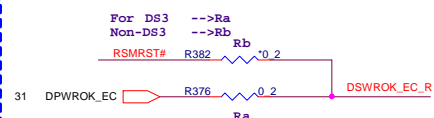




## PCH Pull-high/low(CLG)

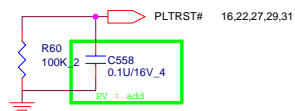


## For DS3 Sequence

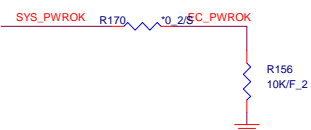
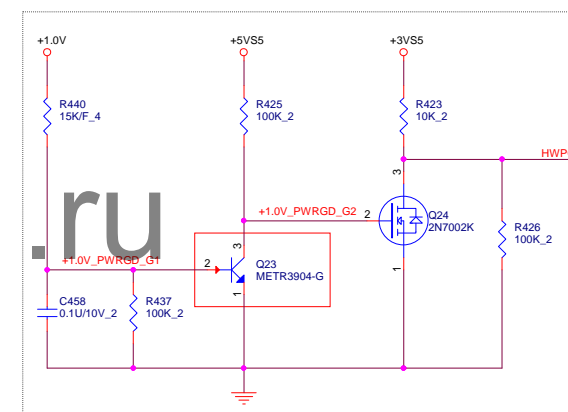
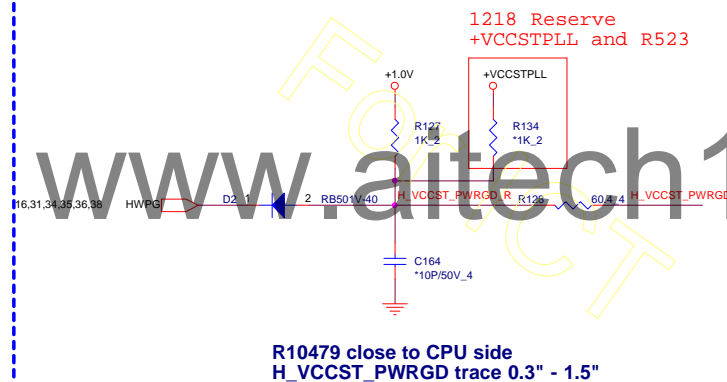


## PLTRST#(CLG)

Check Q2010 Rise/Fall time less than 100ns

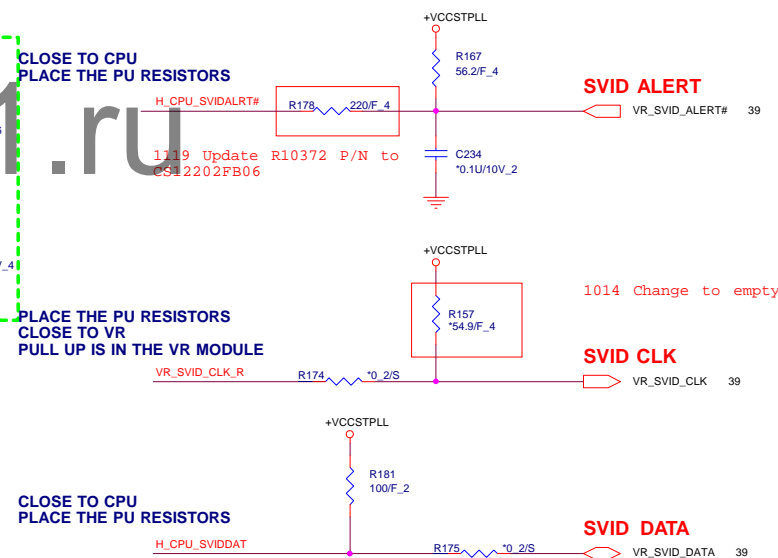
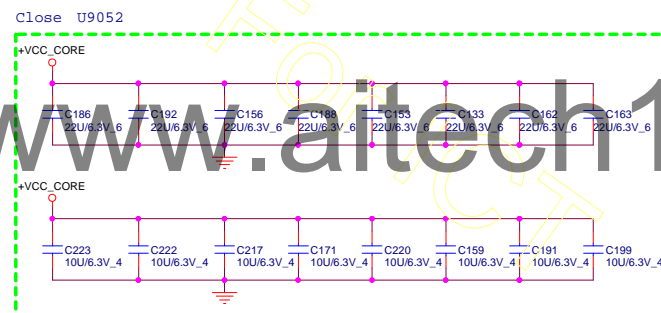


## System PWR\_OK(CLG)

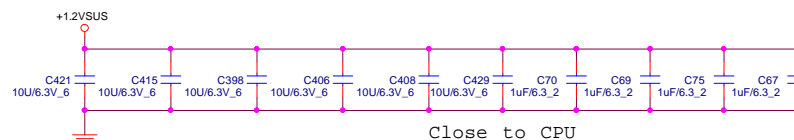
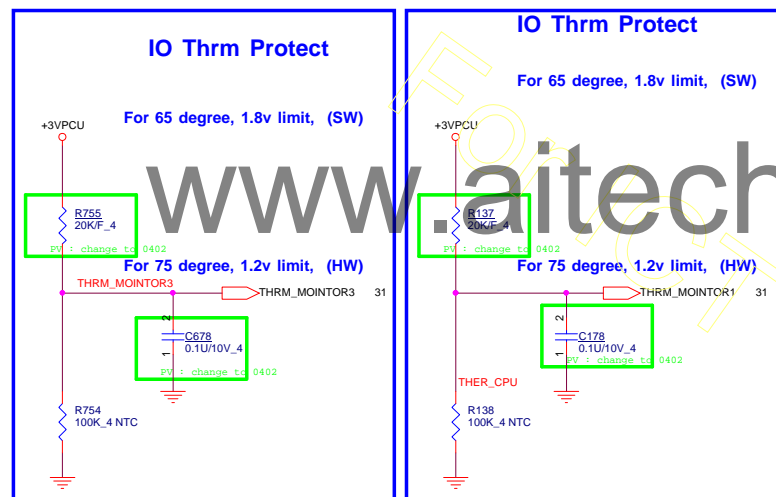
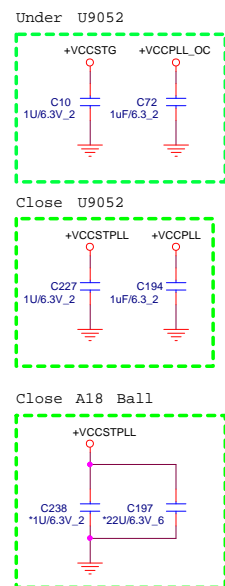
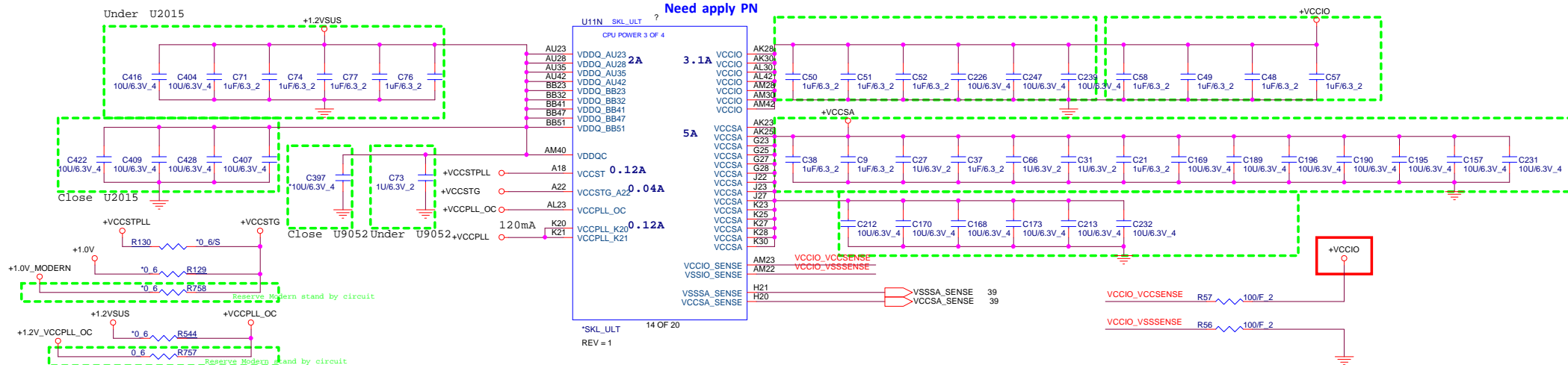
1218 Reserve  
+VCCSTPLL and R523

1110 Add Citcuit for +1.0V Power Good

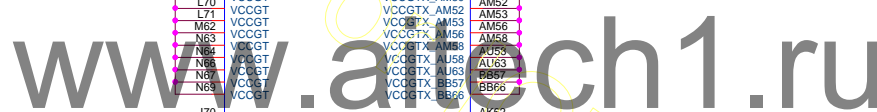
1118 Change Change Q7062 P/N from BA051440000 to  
BA039040020, Del D7002,D7003, R10526, R10527




Power Rail	Description	Control
V <sub>CC</sub>	Processor IA Cores Power Rail	SVID
V <sub>CCGT</sub>	Processor Graphics Power Rails	SVID
V <sub>CCGTx</sub>	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
V <sub>CCSA</sub>	System Agent Power Rail	SVID/Fixed (SKU dependent)
V <sub>CCIO</sub>	IO Power Rail	Fixed
V <sub>CCST</sub>	Sustain Power Rail	Fixed
V <sub>CCPLL</sub>	Processor PLLs power rail	Fixed
V <sub>DDQ</sub>	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
V <sub>CCOPC</sub>	Processor OPC power rail (available only in SKU's with OPC)	Fixed
V <sub>CCOPC_1P8</sub>	Processor OPC power rail (available only in SKU's with OPC)	Fixed
V <sub>CCEOPIO</sub>	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed

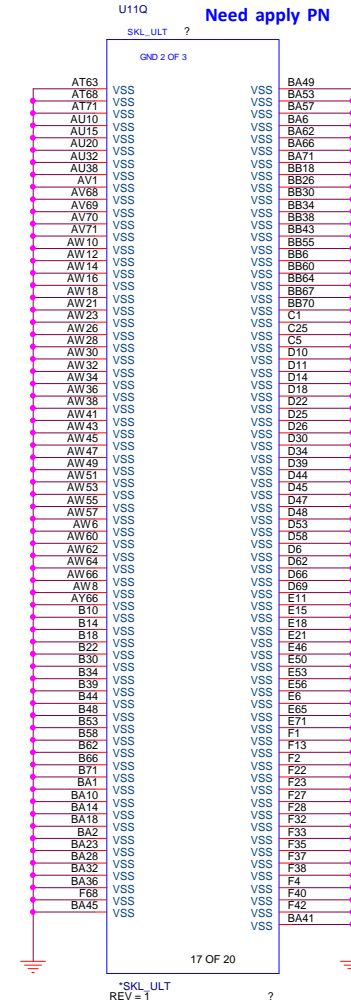
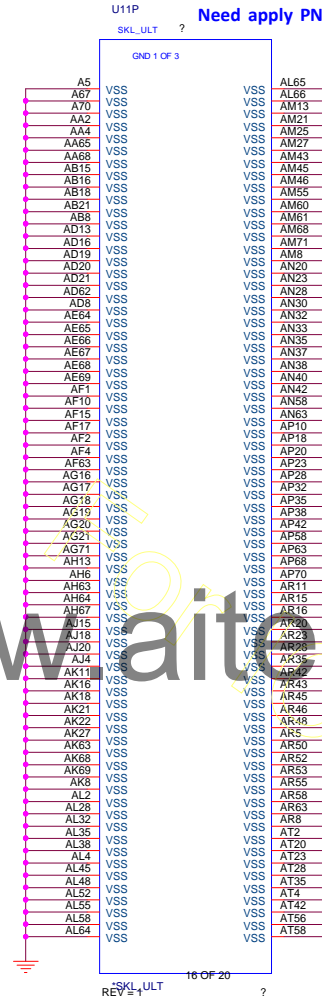
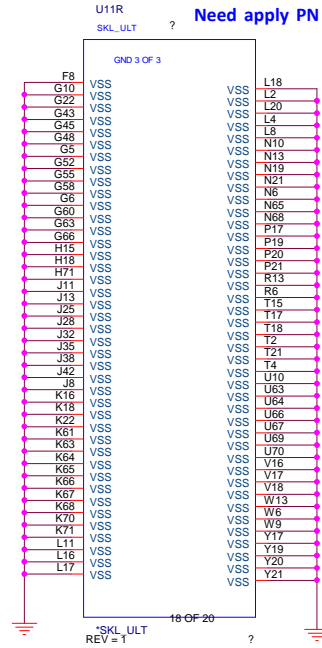


Power Rail	Description	Control
V <sub>CC</sub>	Processor IA Cores Power Rail	SVID
V <sub>CCGT</sub>	Processor Graphics Power Rails	SVID
V <sub>CCGTX</sub>	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
V <sub>CCSA</sub>	System Agent Power Rail	SVID/Fixed (SKU dependent)
V <sub>CCIO</sub>	IO Power Rail	Fixed
V <sub>CCST</sub>	Sustain Power Rail	Fixed
V <sub>CCPLL</sub>	Processor PLLs power rail	Fixed
V <sub>DDQ</sub>	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
V <sub>CCOPC</sub>	Processor OPC power rail (available only in SKU's with OPC)	Fixed
V <sub>CCOPC_1P8</sub>	Processor OPC power rail (available only in SKU's with OPC)	Fixed
V <sub>CCEOPIO</sub>	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed

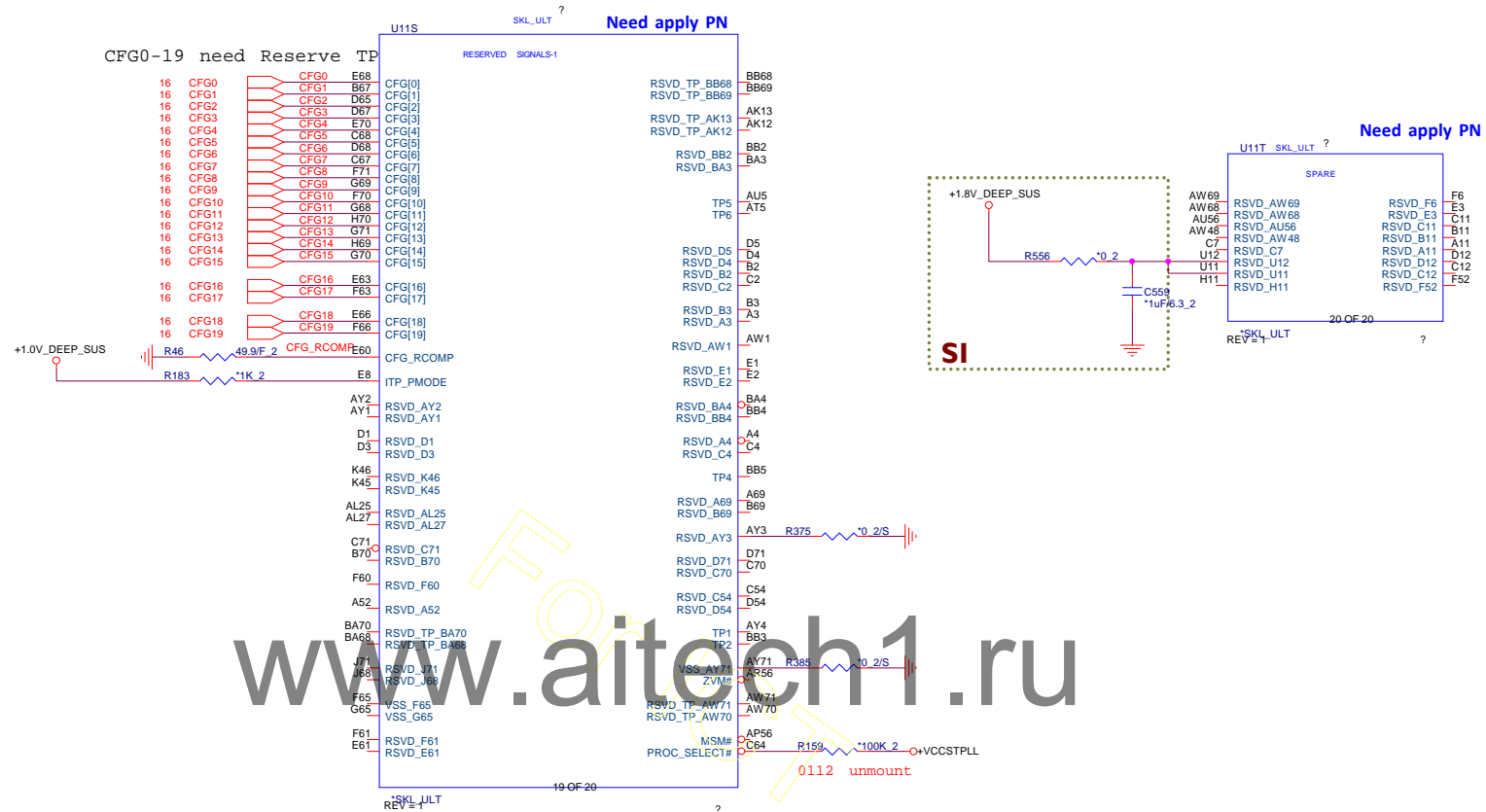


	<b>PROJECT : Pegasus</b> <b>Quanta Computer Inc.</b>		
	Size Custom	Document Number <b>SKL U (6/14)</b>	Rev 1A
	Date: Wednesday, September 30, 2015 Sheet 7 of 44		







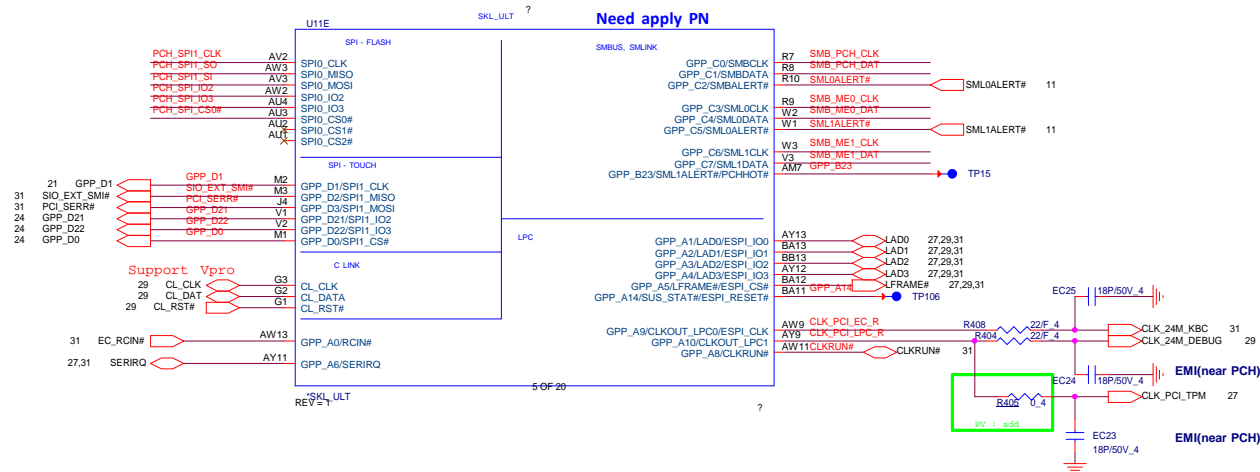


### Processor Strapping

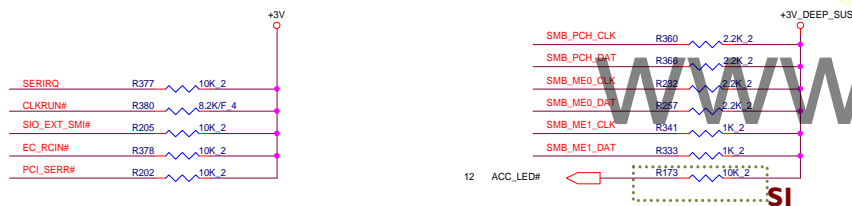
The CFG signals have a default value of '1' if not terminated on the board.

	1	0	Circuit
CFG3 (Physical Debug Enable) DFX_Privacy	Disable:	Enable: Set DFX Enable in DFX interface MSR	CFG3 R143 ~1K 2
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP	CFG4 R42 ~1K 2

+3V\_DEEP\_SUS 4,11,12,14,15,16  
 +3V 2,4,11,12,13,14,15,16,20,21,22,23,24,27,28,30,31,38,39  
 +5V 22,23,24,28,39  
 +1.0V 2,4,5,16,31,37  
 +3VSS 4,15,22,29,31,32,34,36,37,38



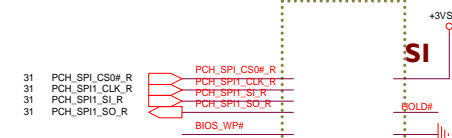
## GPIO Pull UP



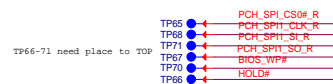
## PCH SPI ROM(CLG)

Vender	Size	P/N	Quanta P/N
EON	8MB	EON EN25QH64-104HIP (QE)	AKE9E2N0001 (EOD)
Winbond	8MB	Winbond W25Q64FVSSIQ (QE)	AKE3EFP0N07
Socket	DFHS08FS023		

## 4M SPI ROM Socket



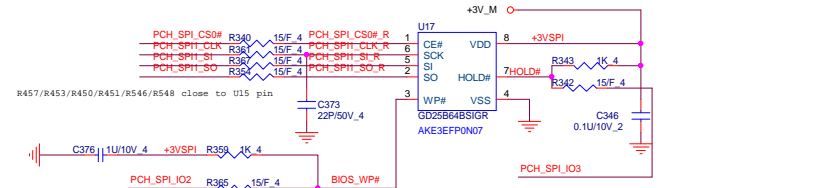
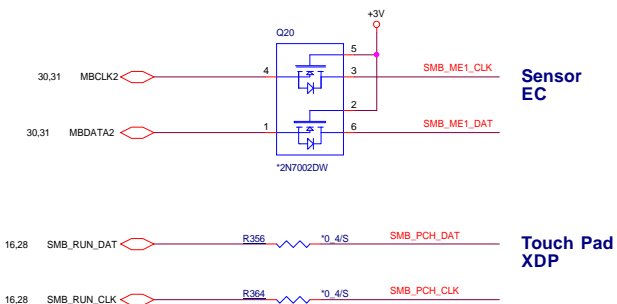
U23&amp;U24 footprint



## PCH SPI ROM(CLG)

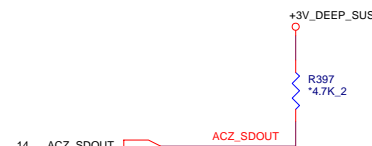
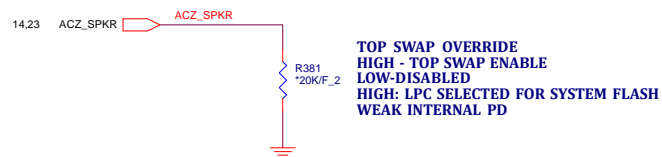
15 +3V\_M

## SMBus/Pull-up(CLG)



# Functional Strap Definitions

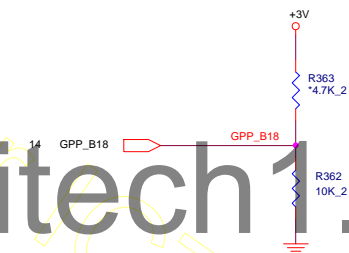
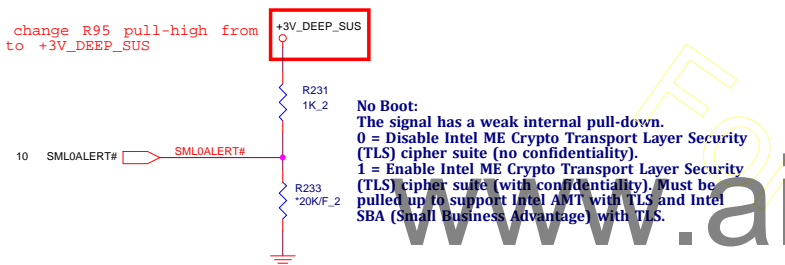
**DESIGN NOTE:**  
WEAK PULL UP RESISTOR PRESENT ON THIS NET



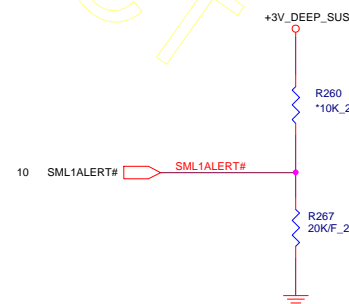
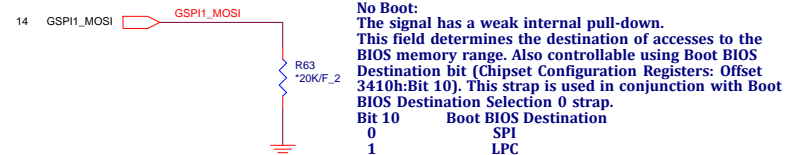
**No Boot:**  
The signal has a weak internal pull-down.  
0 = Enable security measures defined in the Flash Descriptor.  
1 = Disable Flash Descriptor Security (override). This strap should only be asserted high using external pull-up in manufacturing/debug environments ONLY. This function is useful when running ITP/XDP.



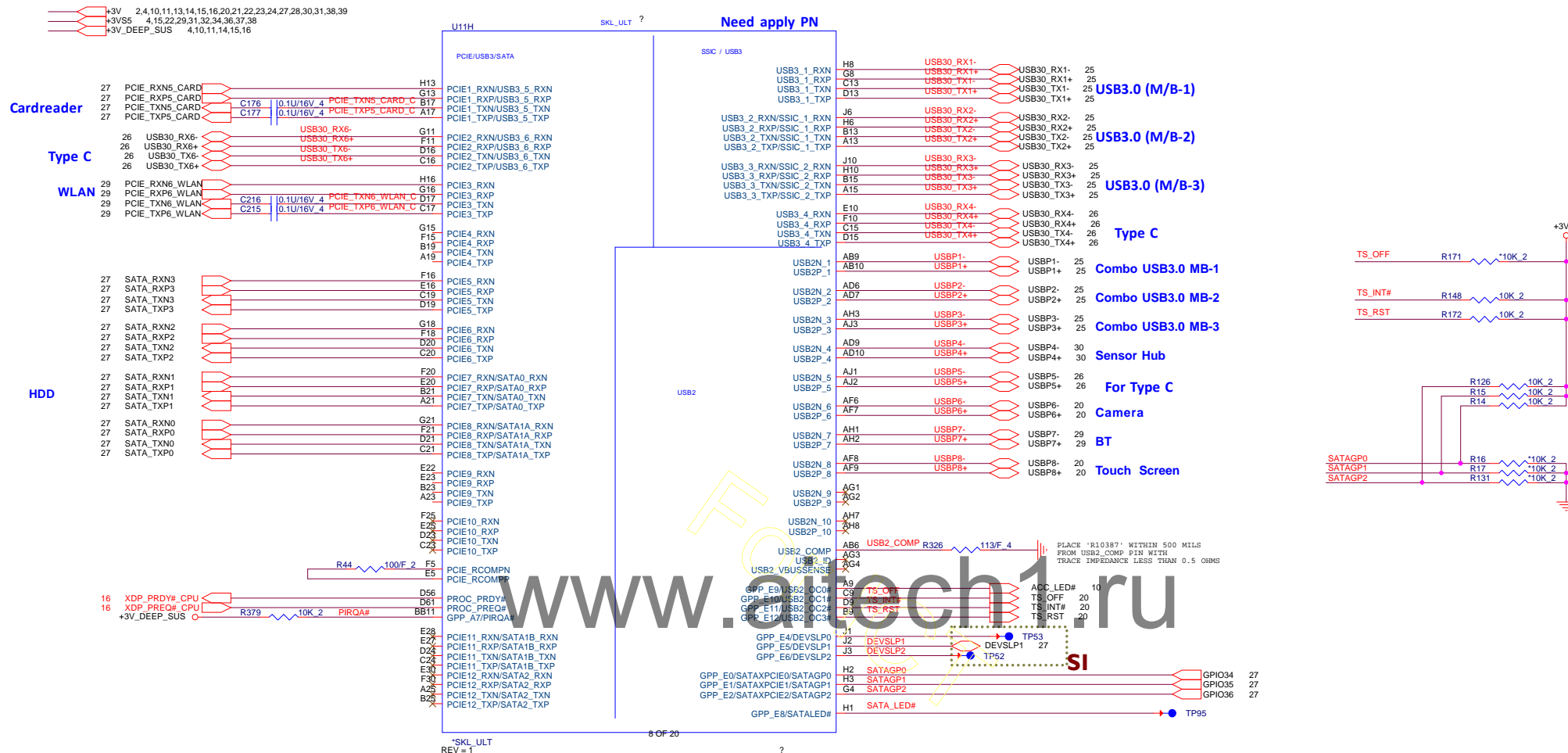
1212 change R95 pull-high from +3V to +3V\_DEEP\_SUS



**No Boot:**  
The signal has a weak internal pull-down.  
0 = Disable No Reboot mode.  
1 = Enable No Reboot mode (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP.



**No Boot:**  
The signal has a weak internal pull-down.  
0 = LPC is selected for EC.  
1 = eSPI is selected for EC.



PCI-E Port Mapping Table

PCI-E Port	Function	CLK RQ Port	Function
Port1	CardReader	Port0	Un-used
Port2	WLAN	Port1	CardReader
Port3	Un-used	Port2	WLAN
Port4	Un-used	Port3	Un-used
Port5	SSD	Port4	Un-used
Port6	SSD	Port5	SSD
Port7	SSD		
Port8	SSD		
Port9	Un-used		
Port10	Un-used		

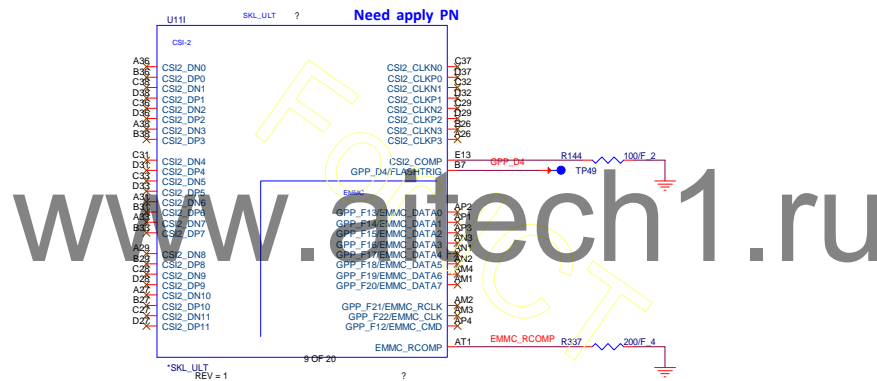
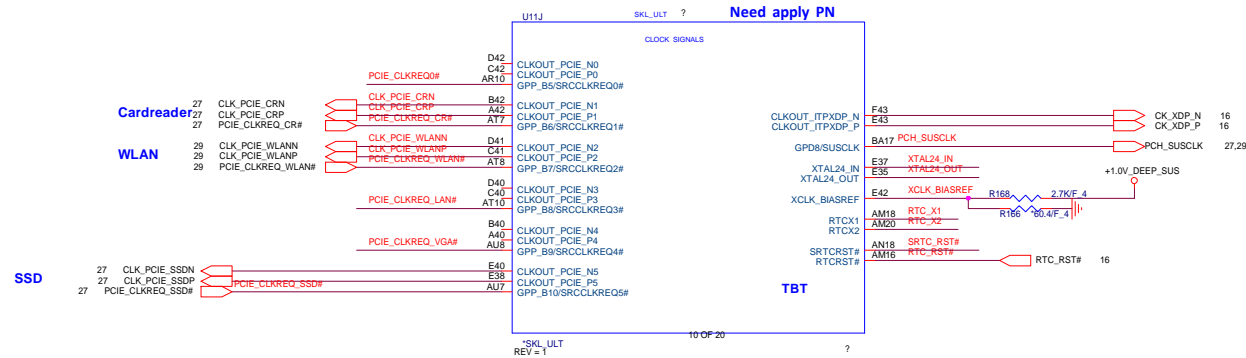
USB3.0 Port Mapping Table

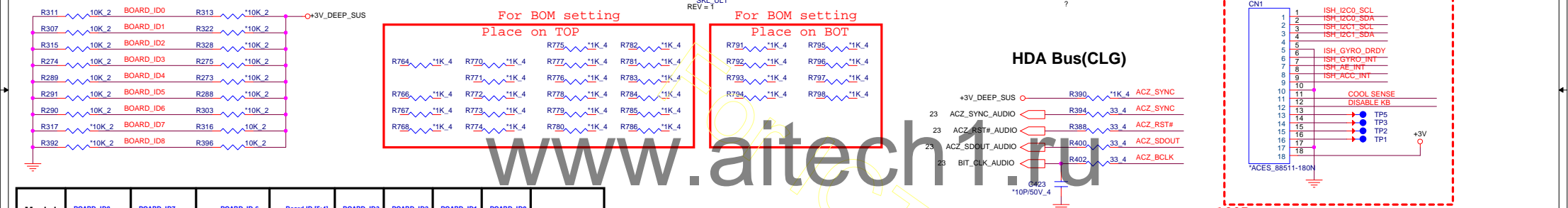
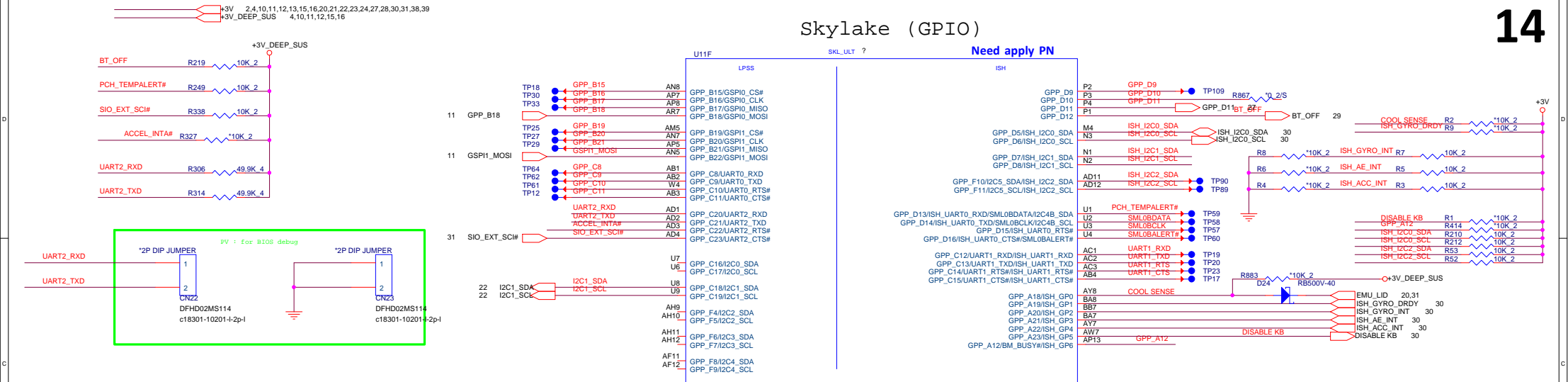
USB3.0	Function
PORT-1	USB3.0 MB-1
PORT-2	USB3.0 MB-2
PORT-3	USB3.0 MB-3
PORT-4	NC

USB2.0 Port Mapping Table

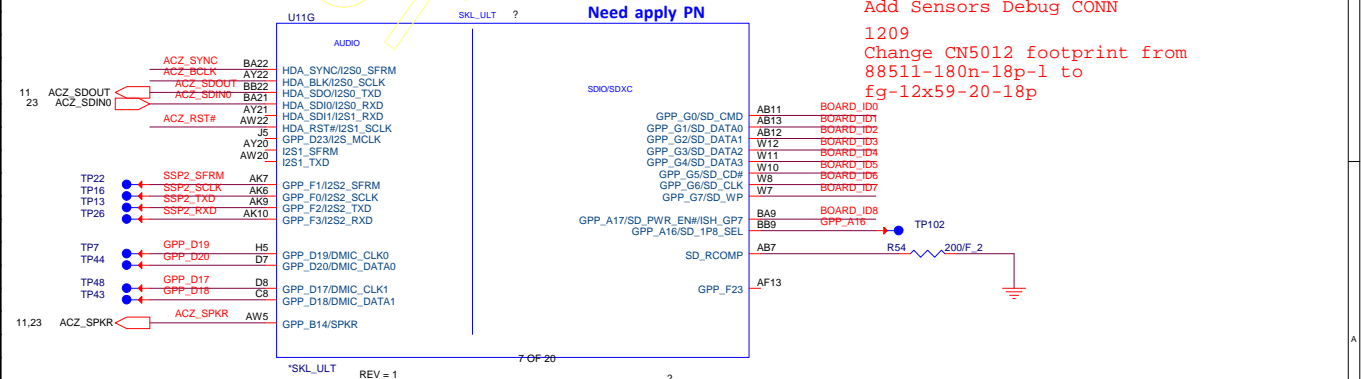
USB2.0	Function
PORT-1	USB3.0 MB-1
PORT-2	USB3.0 MB-2
PORT-3	USB3.0 MB-3
PORT-4	Sensor Hub
PORT-5	NC
PORT-6	Camera
PORT-7	WLAN
PORT-8	Touch Screen
PORT-9	NC
PORT-10	NC

1.8V\_DEEP\_SUS 9,15,36,38  
3V 2,4,10,11,12,14,15,16,20,21,22,23,24,27,28,30,31,38,39





Model	BOARD_ID8	BOARD_ID7	BOARD_ID 6	Board ID [5-4]	BOARD_ID3	BOARD_ID2	BOARD_ID1	BOARD_ID0	
Y0M	0:VPRO 1:non-VPRO	0:Non-IRIS 1:IRIS	Reserve (Default = 00)	Reserve (Default = 00)	0	0	0	0	HYN 4G
					0	0	0	1	SAM 4G
					0	0	1	0	MIC 4G
					0	0	1	1	HYN 8G
					0	1	0	0	SAM 8G
					0	1	0	1	MIC 8G
					0	1	1	0	HYN 12G
					0	1	1	1	HYN 16G
					1	0	0	0	MIC 16G
					1	0	0	1	SAM 16G
					1	0	1	0	
					1	0	1	1	
					1	1	0	0	
					1	1	0	1	
					1	1	1	0	
					1	1	1	1	

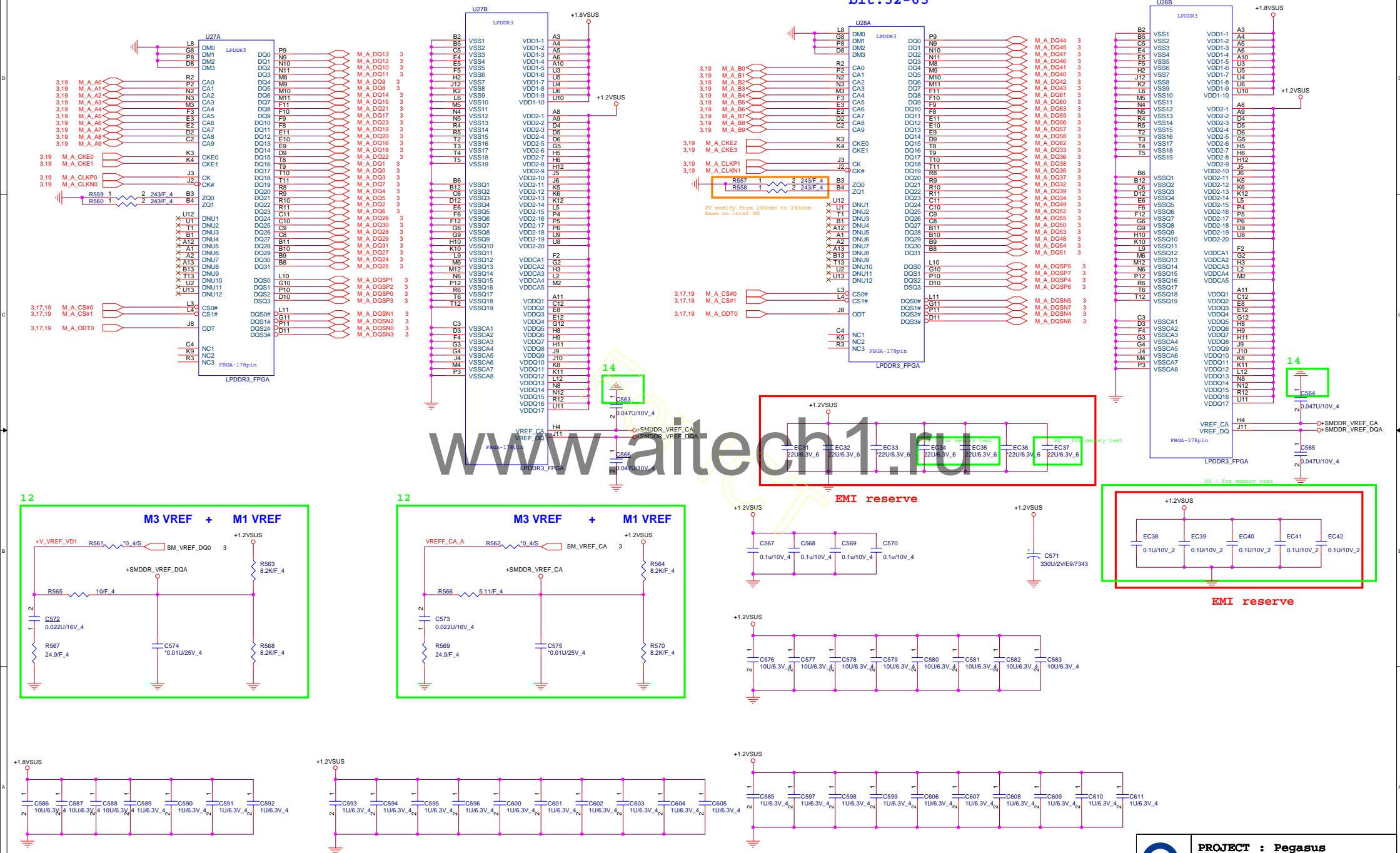






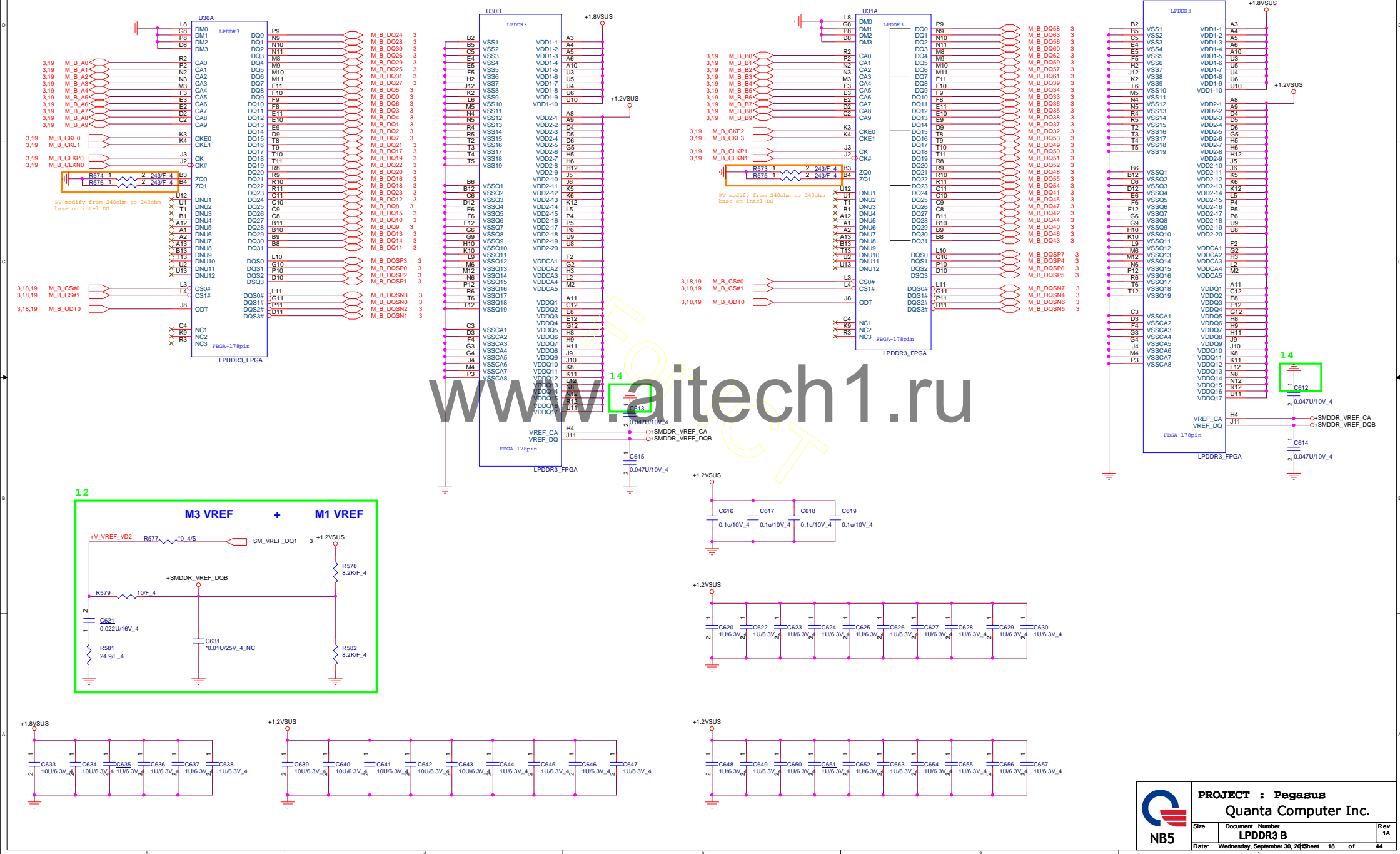


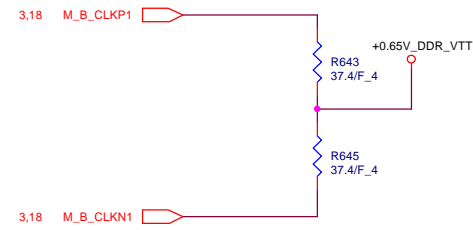
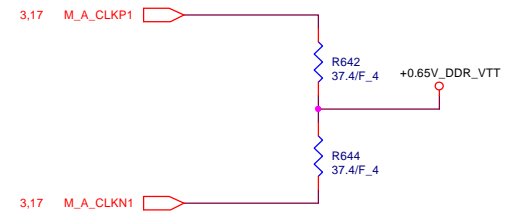
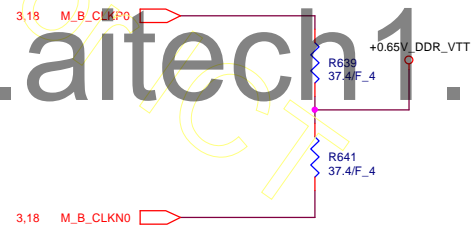
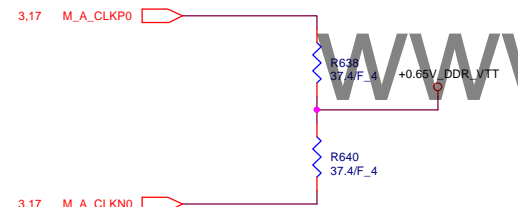
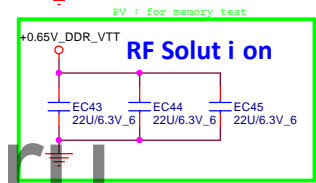
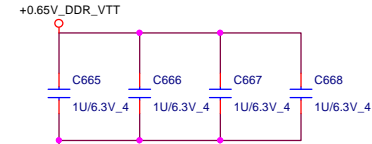
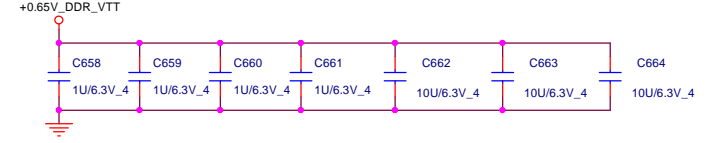
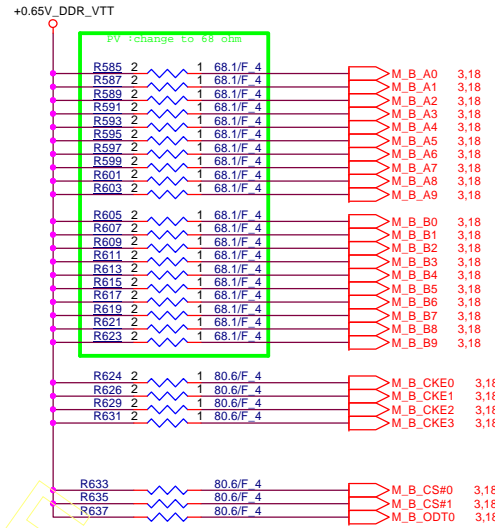
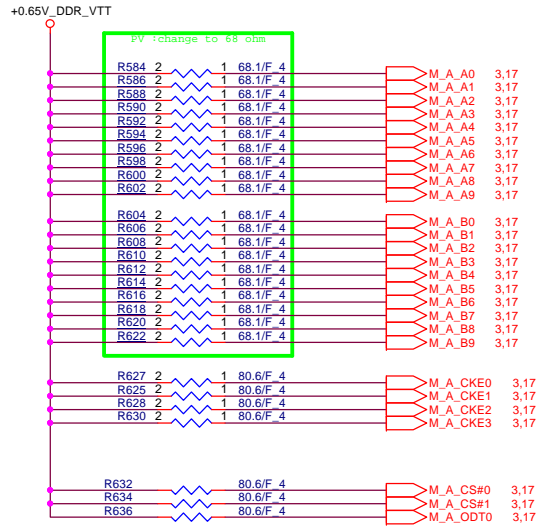
bit:0-31

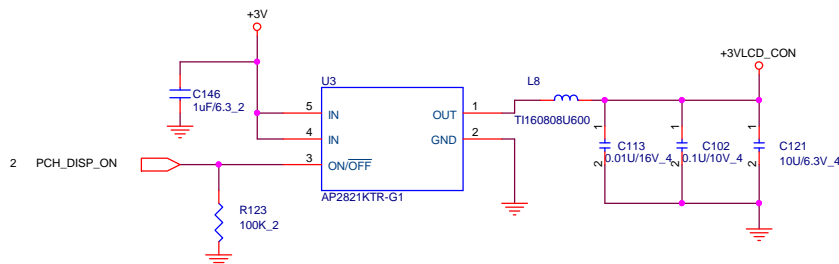
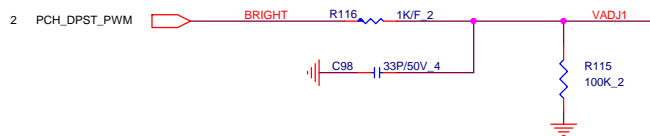
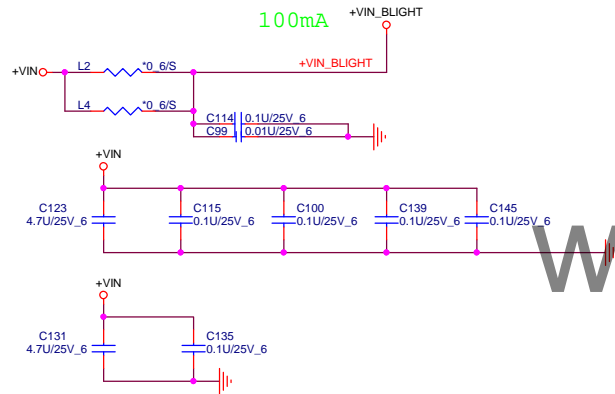
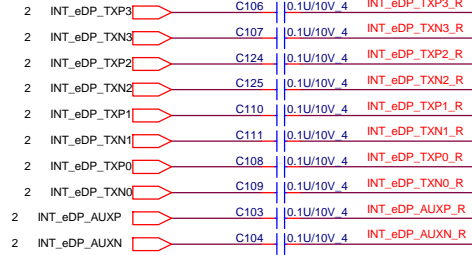
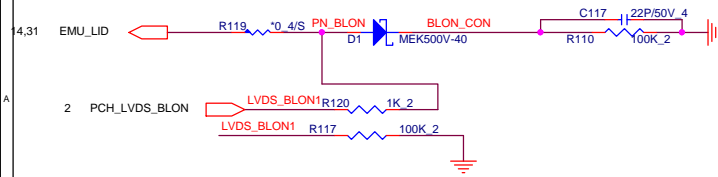


bit:0-31

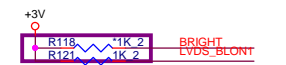
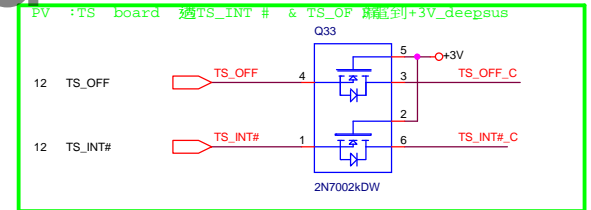
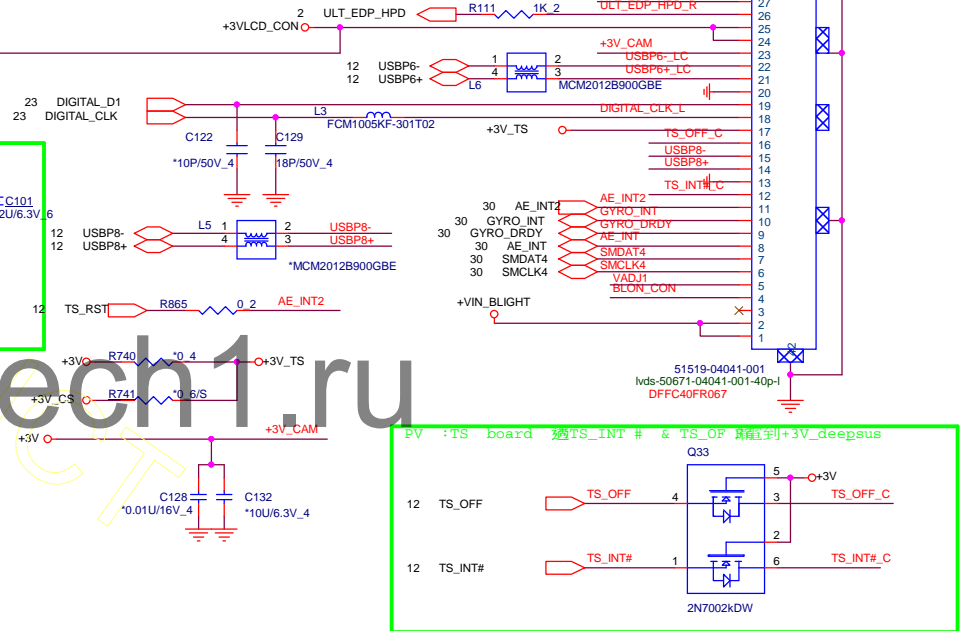
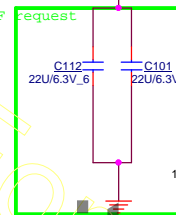
bit:32-63



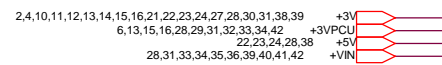




PV :stuff for RF request

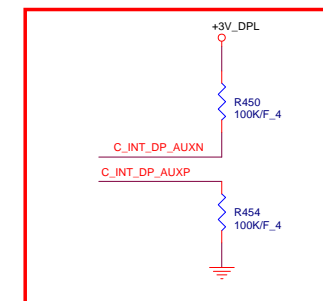
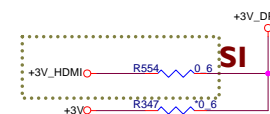


SI modify  
R74 non-stuf f

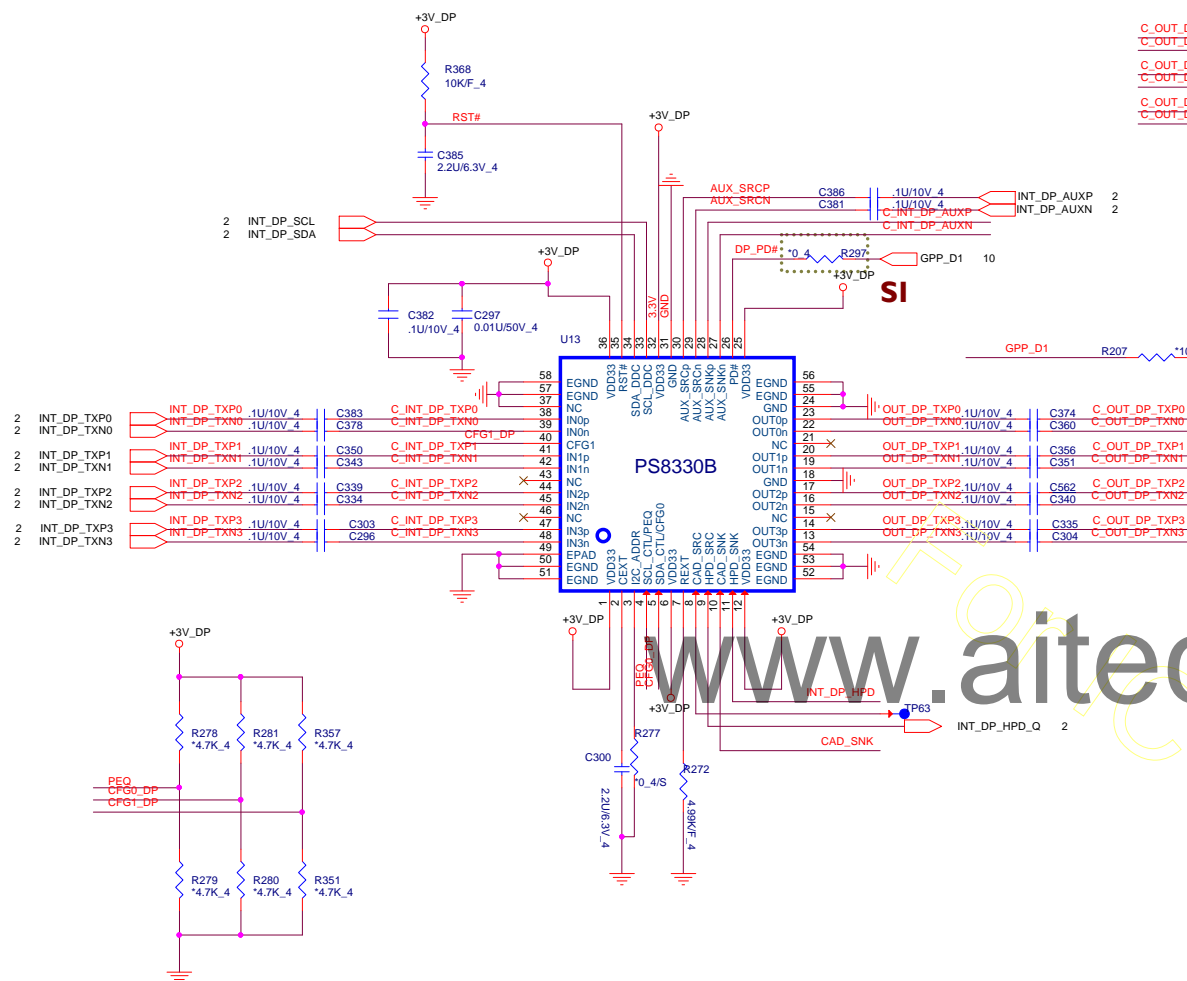


The schematic diagram illustrates the electrical connections for the MAR21-20K5200 module. The module is represented by a blue box with pins 1 through 24. The connections are as follows:

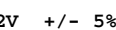
- Mini Display Port (CN15):** Pins 1-20 are connected to the module. Pins 21-24 are connected to the module.
- COUT\_DP Signals:**
  - COUT\_DP\_TXP0 (Pin 1) and COUT\_DP\_TXN0 (Pin 2) are connected to the module.
  - COUT\_DP\_TXP1 (Pin 3) and COUT\_DP\_TXN1 (Pin 4) are connected to the module.
  - COUT\_DP\_TXP2 (Pin 5) and COUT\_DP\_TXN2 (Pin 6) are connected to the module.
  - COUT\_DP\_TXP3 (Pin 7) and COUT\_DP\_TXN3 (Pin 8) are connected to the module.
  - C.INT\_DP\_AUXP (Pin 9) and C.INT\_DP\_AUXN (Pin 10) are connected to the module.
- INT\_DP Signals:**
  - INT\_DP\_HPDP (Pin 11) and CAD\_SNK (Pin 12) are connected to the module.
  - INT\_DP\_AUXP (Pin 13) and INT\_DP\_AUXN (Pin 14) are connected to the module.
- Power Supply:**
  - +3V\_DPL (Pin 15) is connected to the module.
  - +3V\_DP (Pin 16) is connected to the module.
  - +3V\_DP (Pin 17) is connected to the module.
  - +3V\_DP (Pin 18) is connected to the module.
  - +3V\_DP (Pin 19) is connected to the module.
  - +3V\_DP (Pin 20) is connected to the module.
  - +3V\_DP (Pin 21) is connected to the module.
  - +3V\_DP (Pin 22) is connected to the module.
  - +3V\_DP (Pin 23) is connected to the module.
  - +3V\_DP (Pin 24) is connected to the module.
- Resistors and Capacitors:**
  - R476 (100K/F) is connected between pins 11 and 12.
  - R464 (1M/F) is connected between pins 13 and 14.
  - R457 (S.1M 4) is connected between pins 15 and 16.
  - C475 (10U/6.3V\_8) is connected between pins 17 and 18.
  - C468 F2 (1U/10V\_4) is connected between pins 19 and 20.
  - FUSE1.1A8V\_POLY (1.1A/6V) is connected between pins 21 and 22.



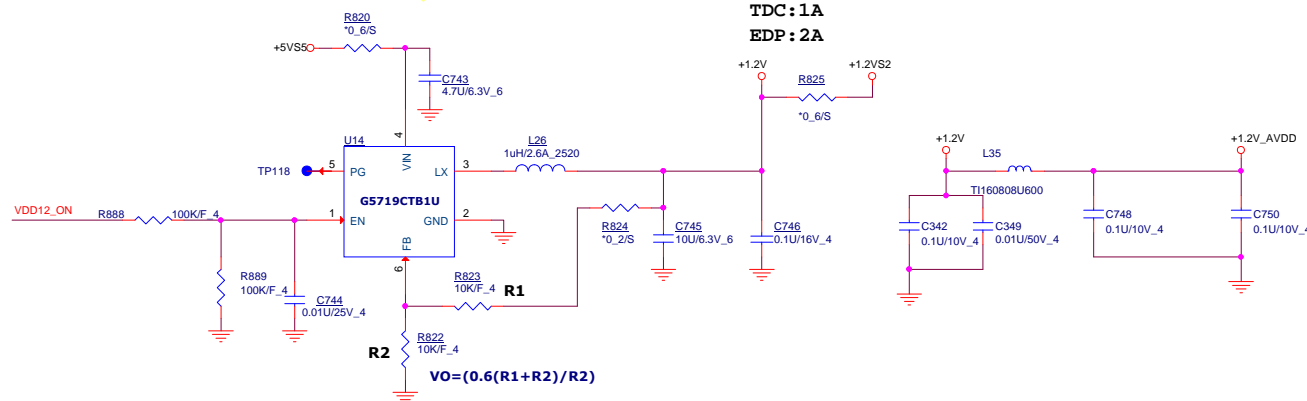
for intel recommend



www.aitech1.ru



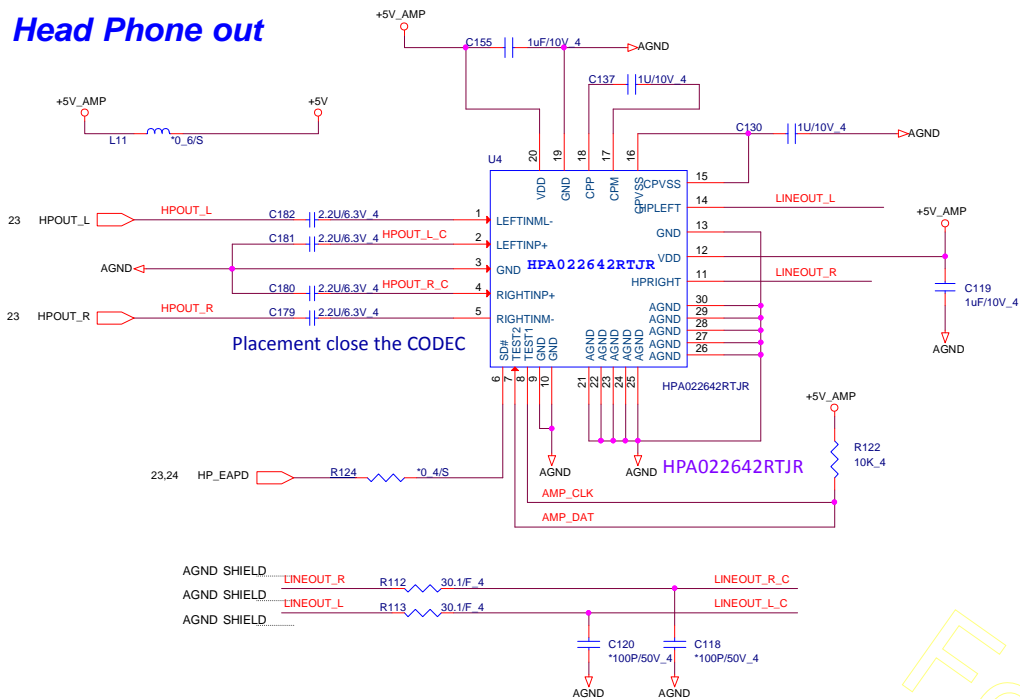
TDC:1A  
EDP:2A



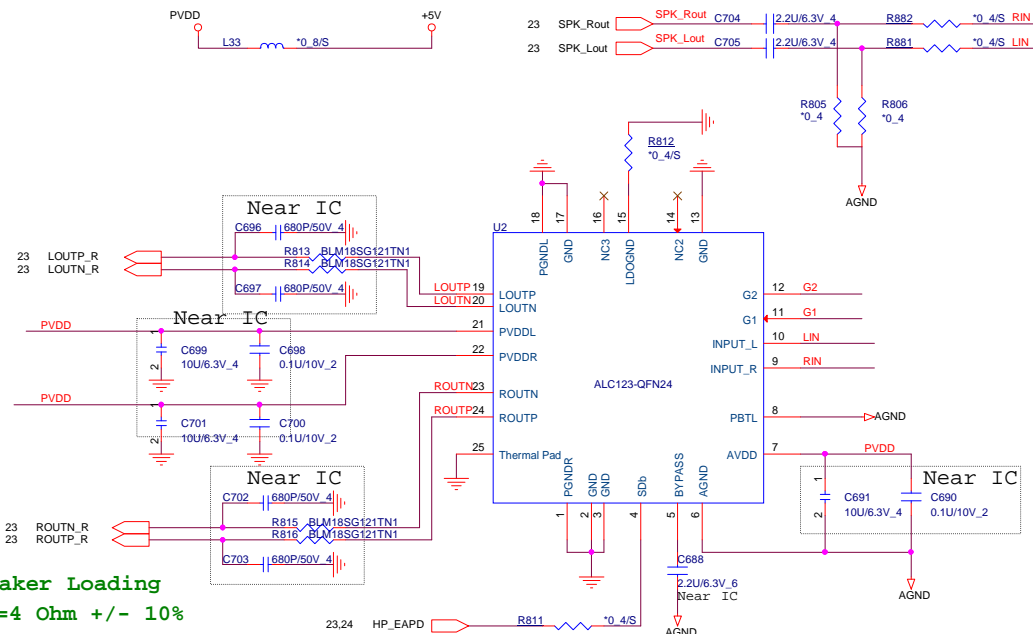




## Head Phone out

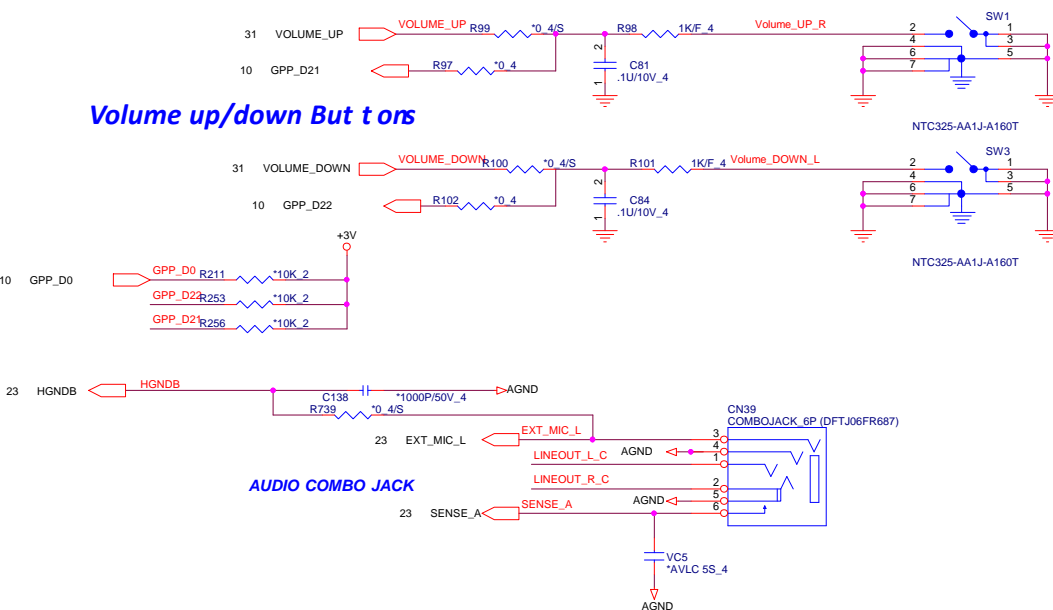


## Speaker out



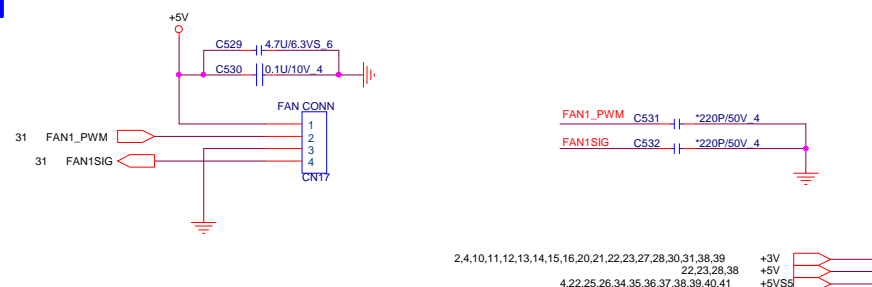
## Audio combo JACK & Volume up/down Buttons

### Volume up/down Buttons



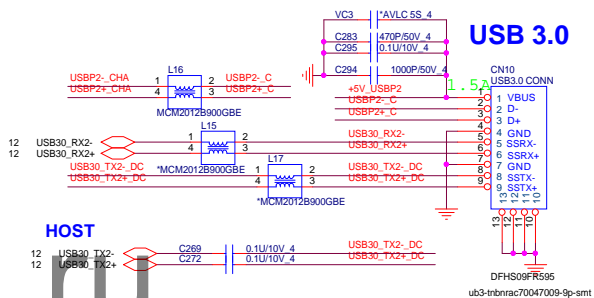
### AUDIO COMBO JACK

## FAN

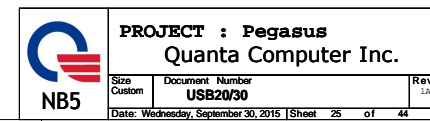


### Fixed Gain Mode Gain Setting

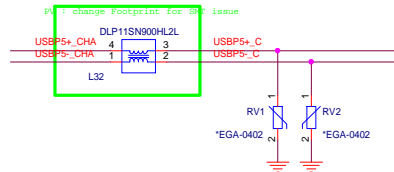
0	0	1 0
0	0	1 0
1	1	1 0
1	0	1 0
1	1	1 0

[illegible]

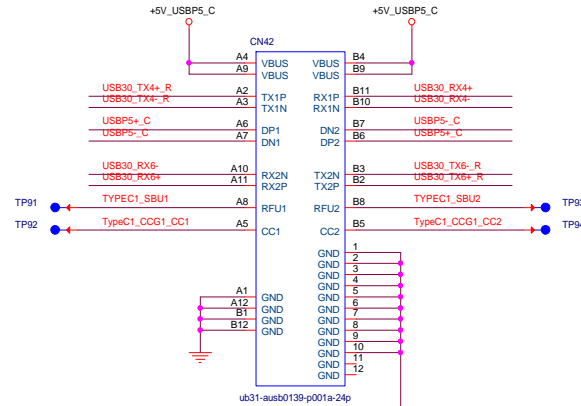
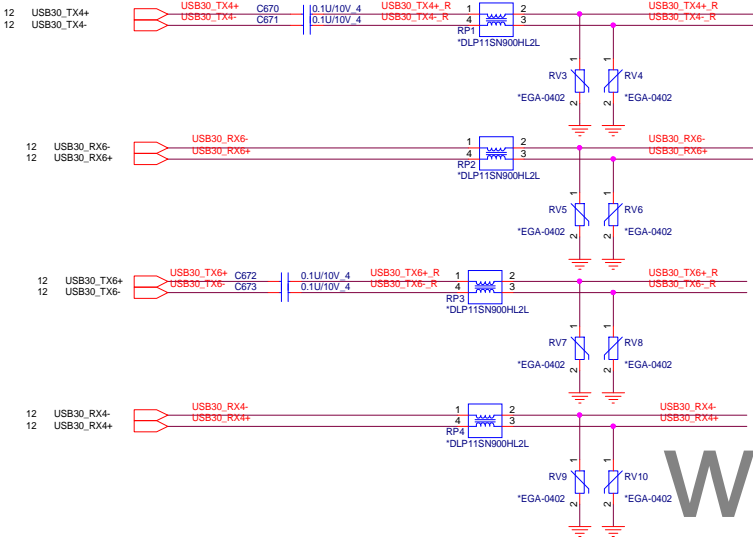
SYSTEM GLOBAL POWER STATE	TPS2546 CHARGING MODE	CTL1	CTL2	CTL3	ILIM_SEL	CURRENT LIMIT SETTING
S0	SDP1	1	1	0	1 or 0	ILIM_HI / ILIM_LO
S0	SDP2, no discharge to / from CDP	1	1	1	0	ILIM_LO
S0	CDP, load detection with ILIM_LO + 60mA thresholds or if a BC1.2 primary detection occurs	1	1	1	1	ILIM_HI
S4/S5	Auto mode, load detection with power wake thresholds	0	0	1	1	ILIM_HI
S3/S4/S5	Auto mode, no load detection	0	0	1	0	ILIM_HI
S3	Auto mode, keyboard/mouse wake up, load detection with ILIM_LO + 60 mA thresholds	0	1	1	1	ILIM_HI
S3	Auto mode, keyboard/mouse wake-up, no load detection	0	1	1	0	ILIM_HI
S3	SDP1, keyboard/mouse wake-up	0	1	0	1 or 0	ILIM_HI / ILIM_LO



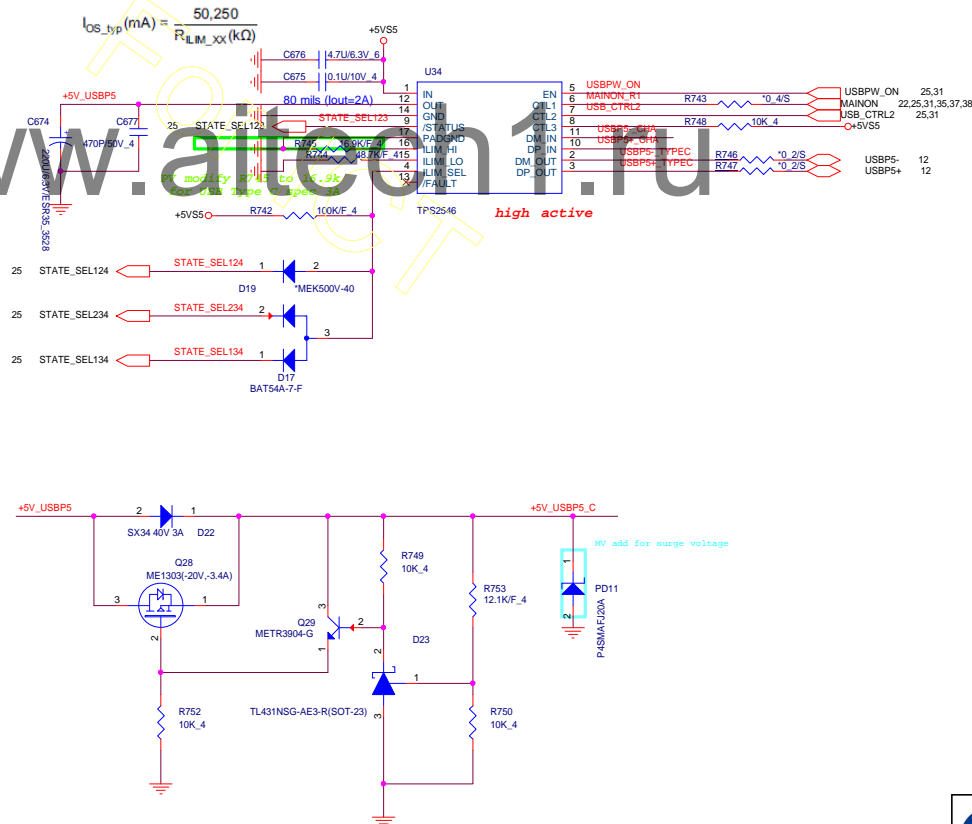
## USB2.0 ESD



## Type C1\_HSIO\_ESD

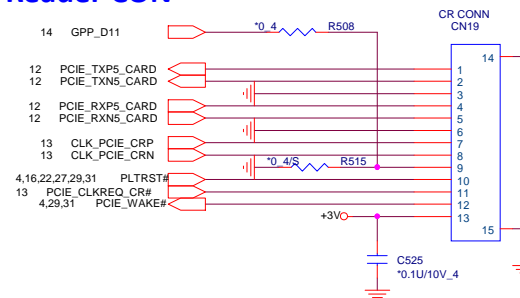


Check P/N &amp; footprint

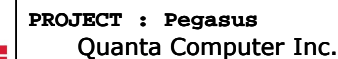




## Card Reader CON

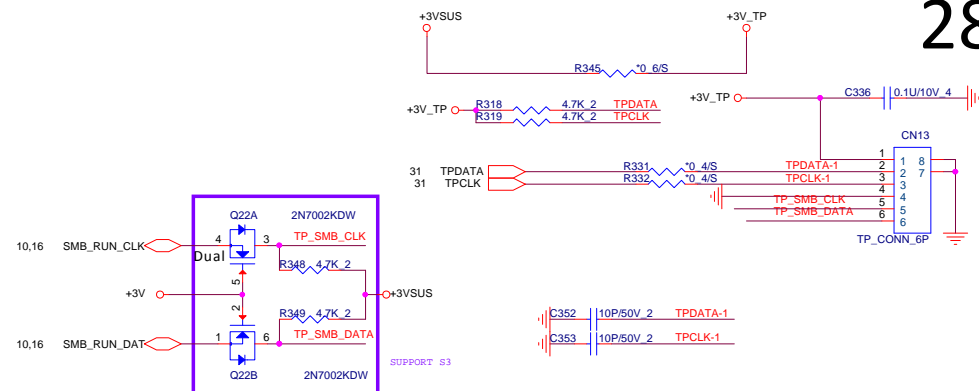
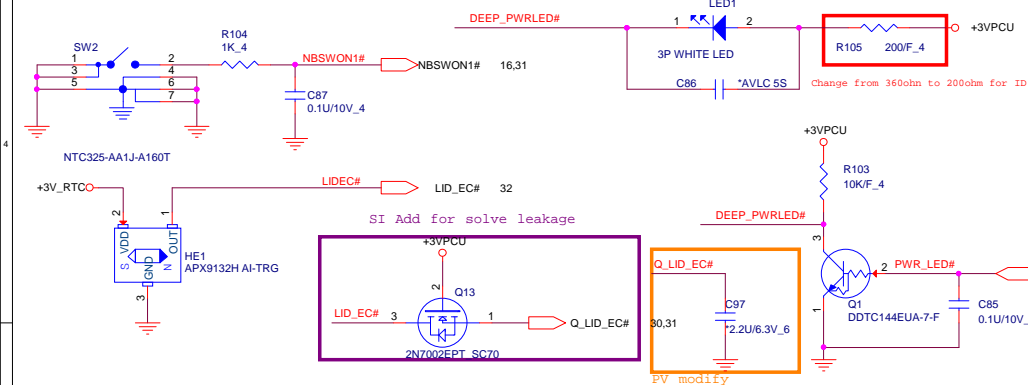


2,4,10,11,12,13,14,15,16,20,21,22,23,24,28,30,31,38,39 +3V  
22,23,24,28,38 +5V  
6,13,15,16,28,29,31,32,33,34,42 +3VPCU

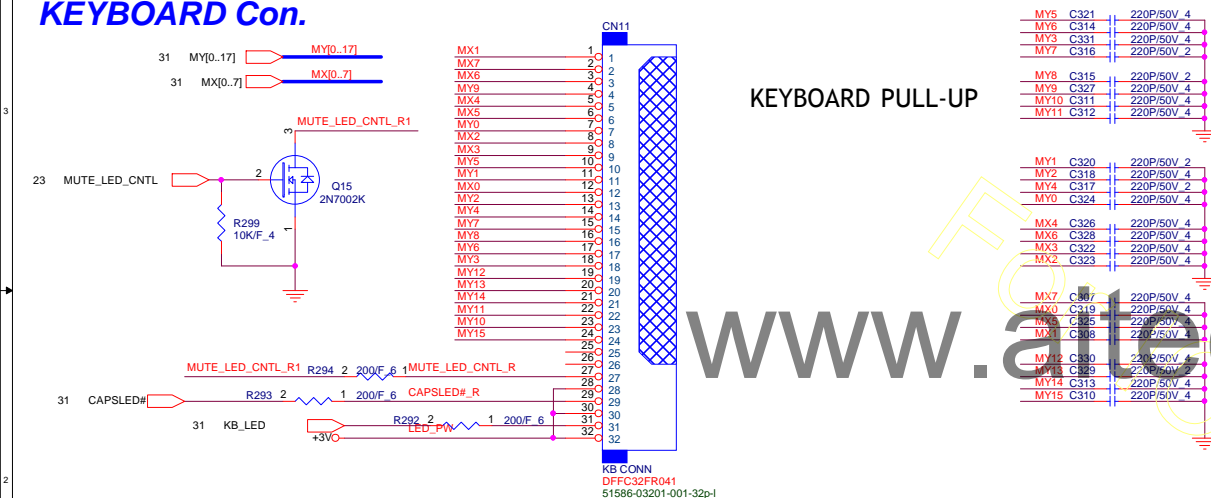


Size Custom	Document Number <b>NGFF HDD/TPM/CR</b>	Rev 1A
Date: Friday, October 02, 2015	Sheet 27 of 42	

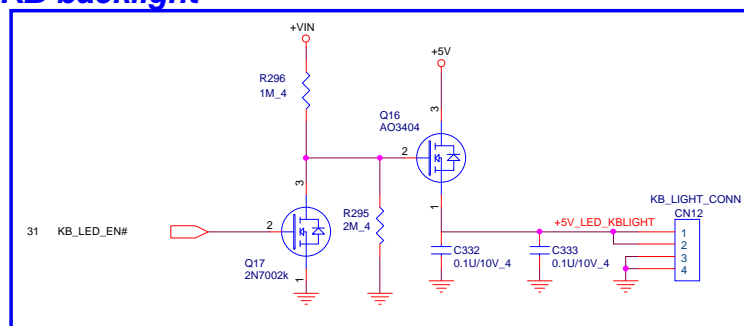
## Power Bot t on



## KEYBOARD Con.



## KB backlight



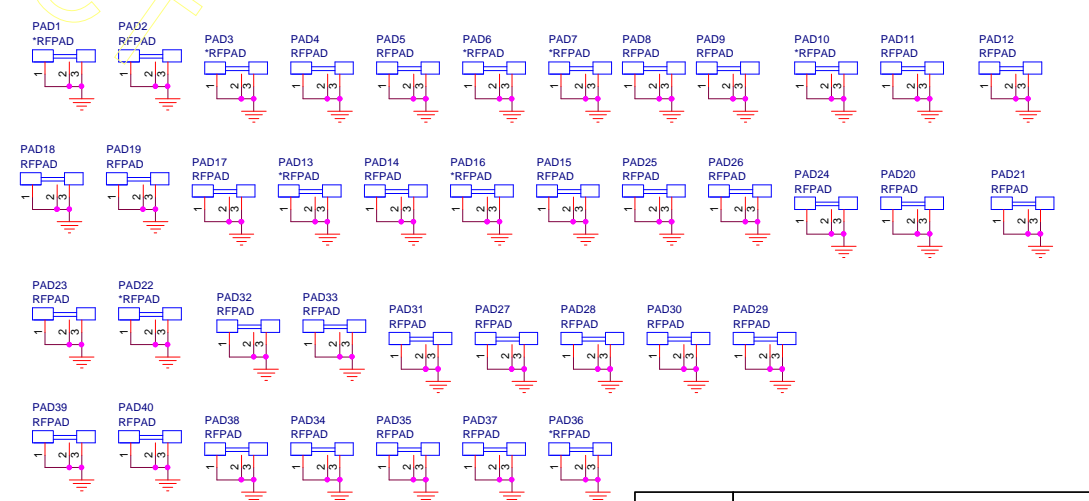
2,4,10,11,12,13,14,15,16,20,21,22,23,24,27,30,31,38,39 +3V


22,23,24,38 +5V

6,13,15,16,29,31,32,33,34,42 +3VPCU

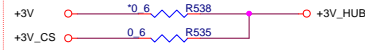
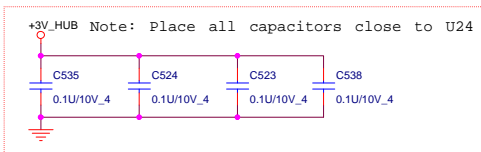


GND Clipse



 <b>NB5</b>	<b>PROJECT : Pegasus</b> <b>Quanta Computer Inc.</b>		
	Size Custom	Document Number <b>WLANHOLE</b>	Rev 1A
Date: Friday, October 02, 2015		Sheet 29 of 42	

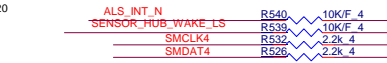




please ST strap setting guideline  
PA1 ~ PA3 --> G + E-compass  
PA4 ~ PA6--> Gyro

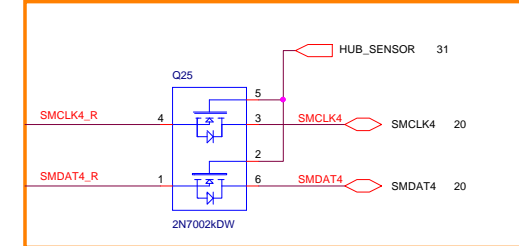
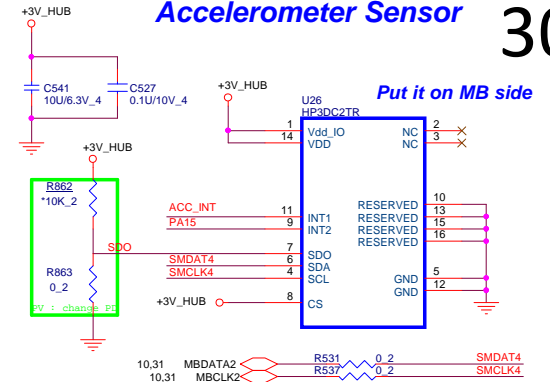
Gyro/G-sensor /  
E-compass  
orientation  
strapping

To G-sensor  
To Gyro sensor



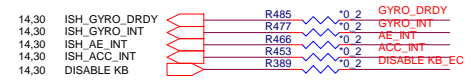
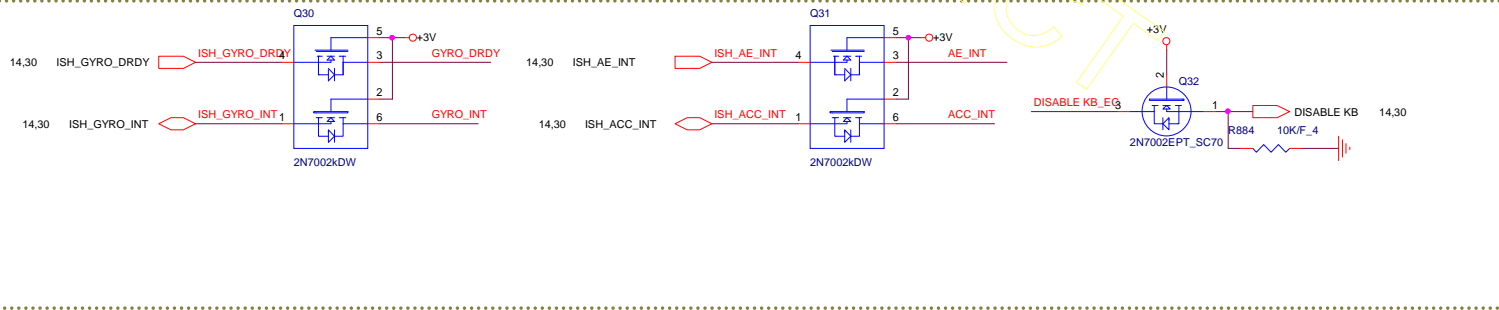
# Accelerometer Sensor 30

Put it on MB side

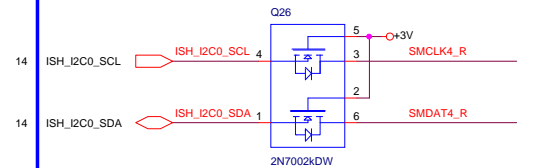
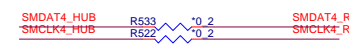


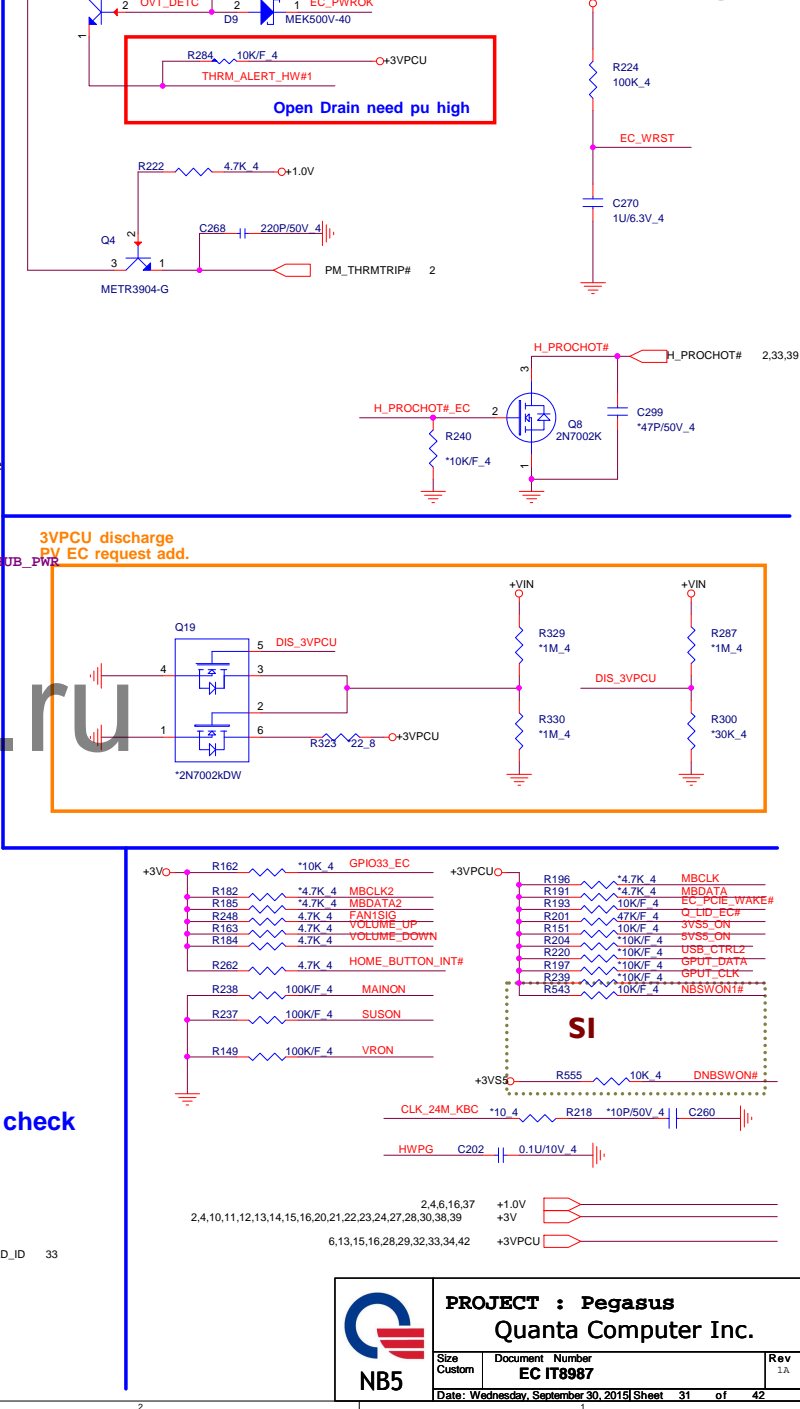
PV add for EC request

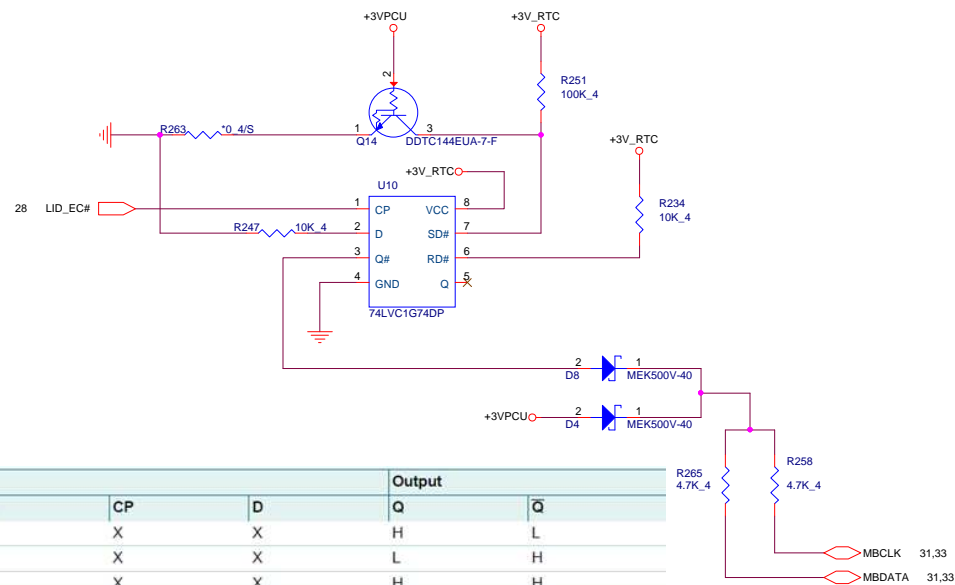
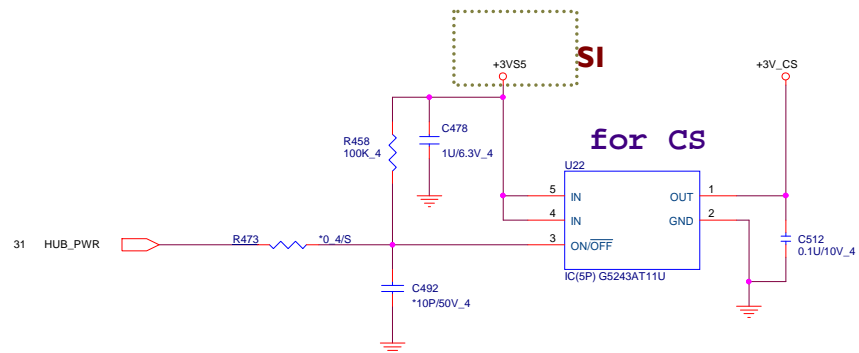
www.aitech1.ru



To Sensor Hub SMBUS





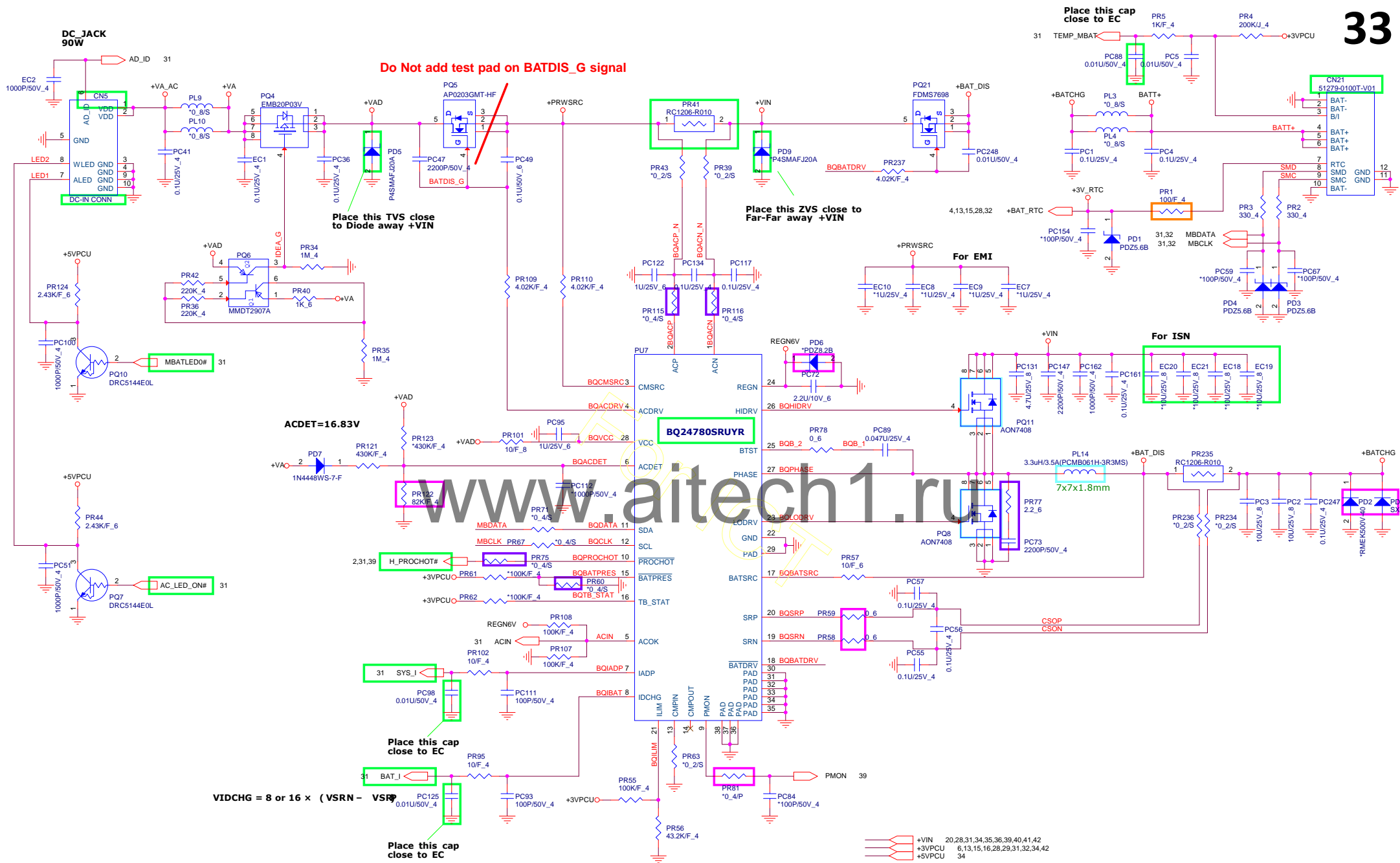


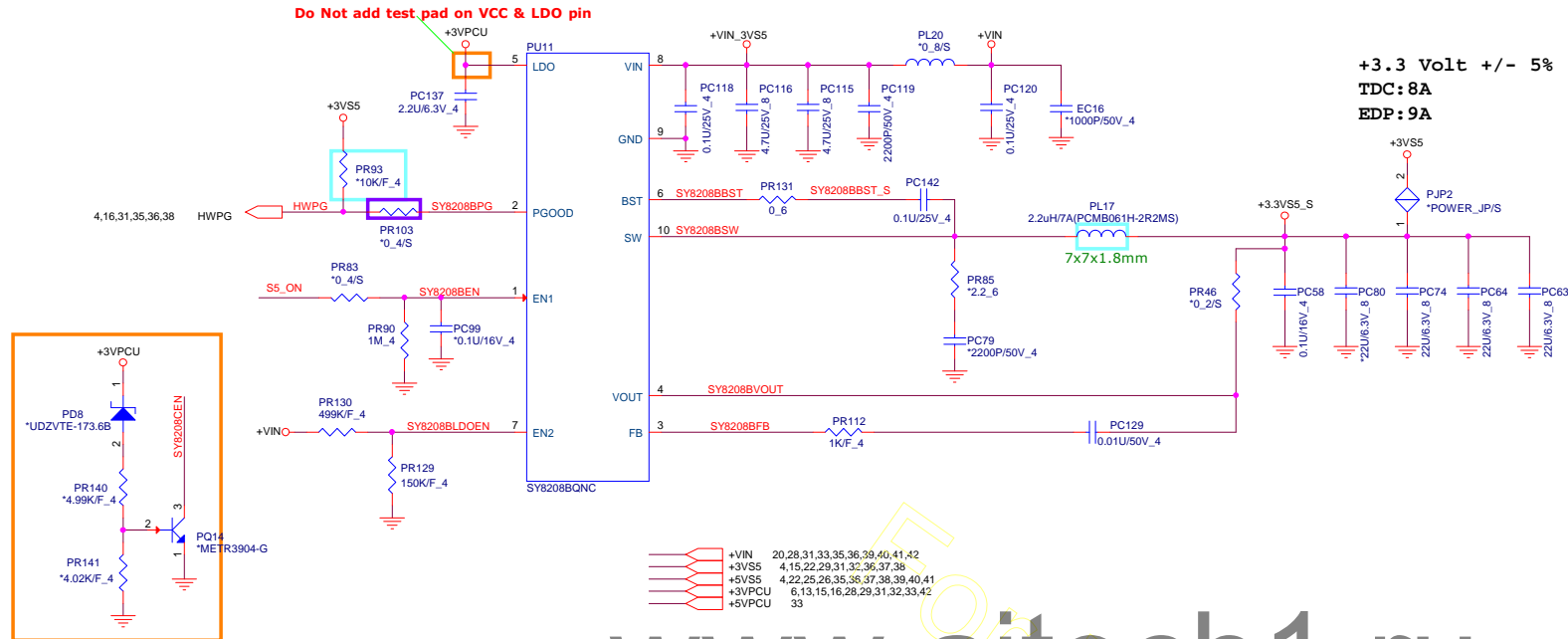
Input				Output	
SD	RD	CP	D	Q	Q̄
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H	H

[1] H = HIGH voltage level;  
L = LOW voltage level;  
X = don't care.

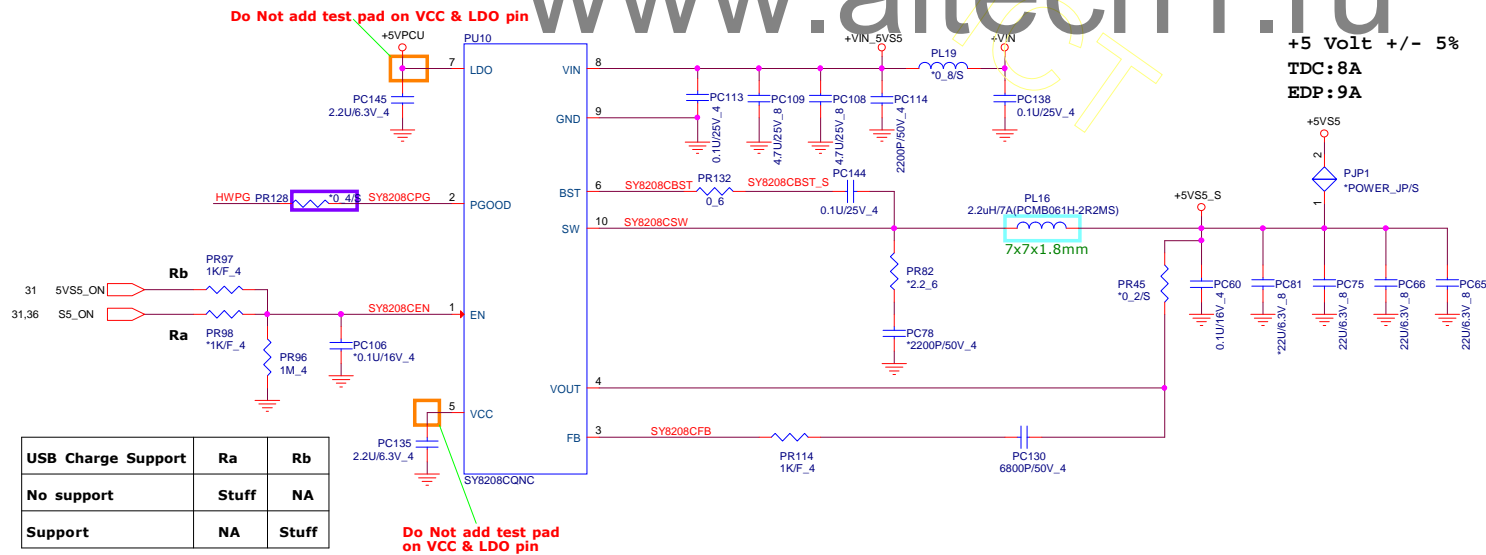
Input				Output	
SD	RD	CP	D	Q <sub>n+1</sub>	Q̄ <sub>n+1</sub>
H	H	↑	L	L	H
H	H	↑	H	H	L

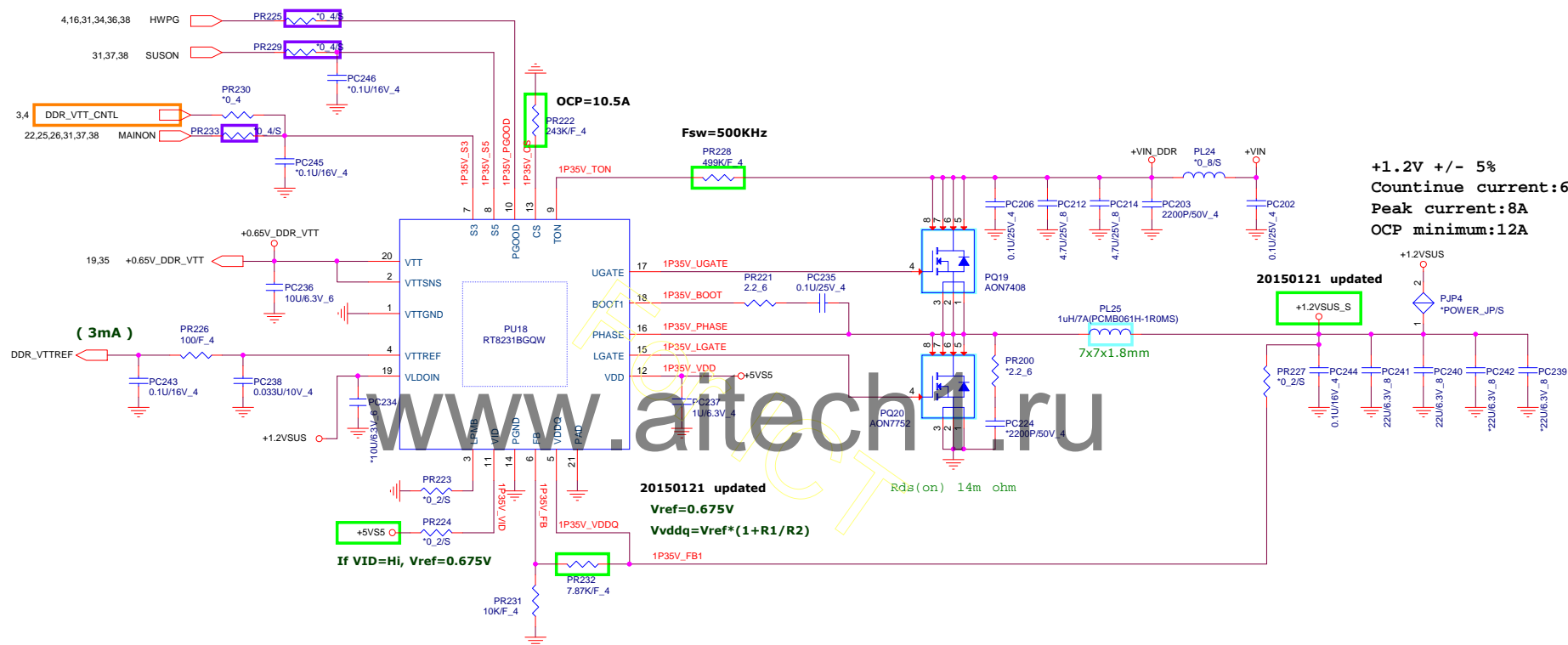
[1] H = HIGH voltage level;  
L = LOW voltage level;  
↑ = LOW-to-HIGH CP transition;  
Q<sub>n+1</sub> = state after the next LOW-to-HIGH CP transition.





www.aitech1.ru

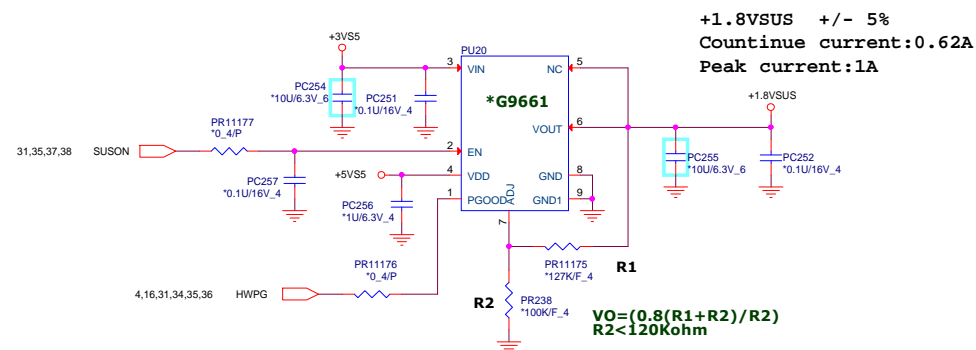
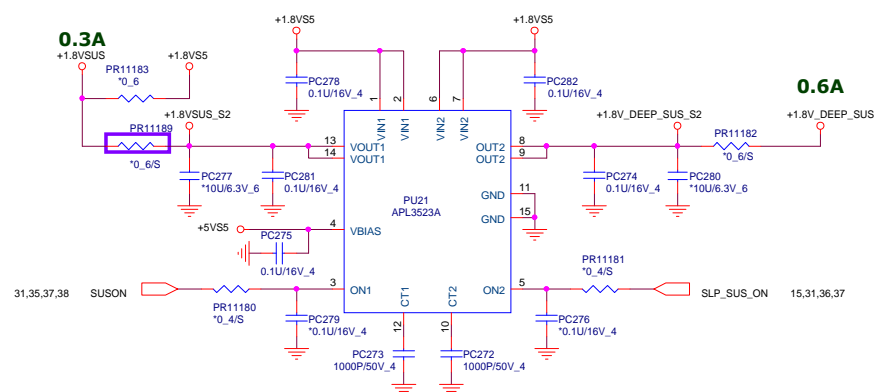
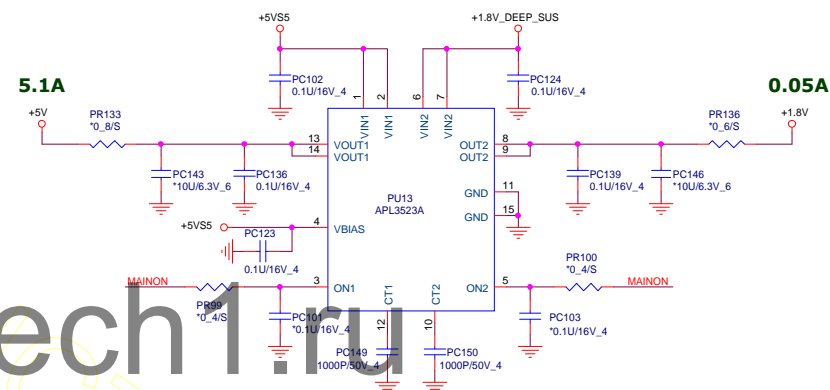
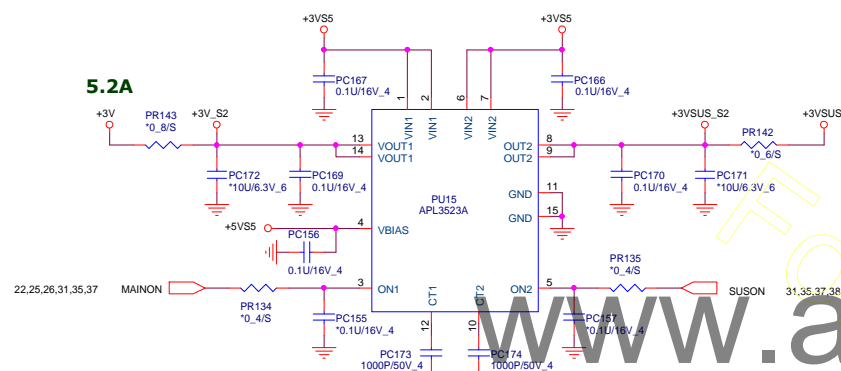


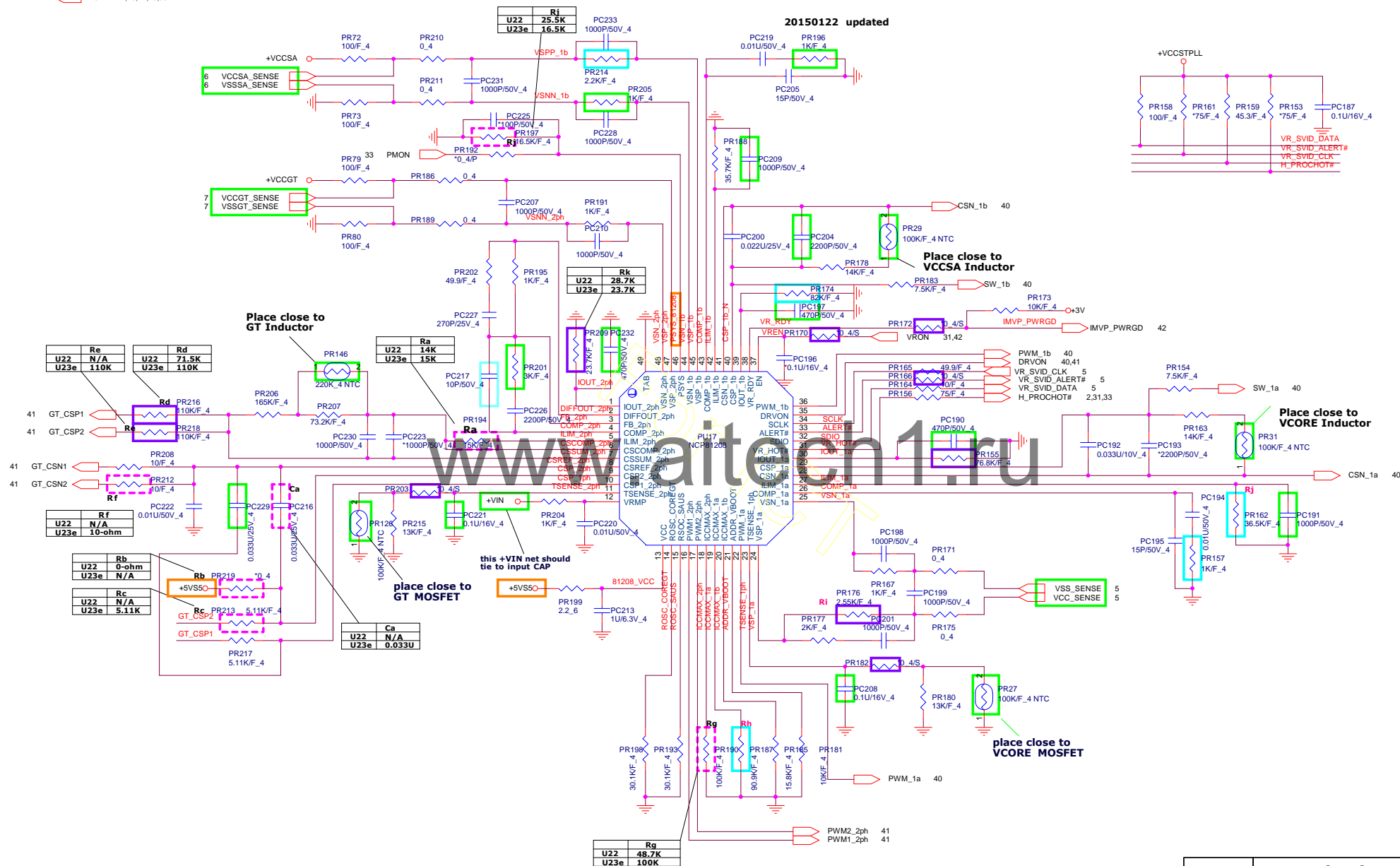




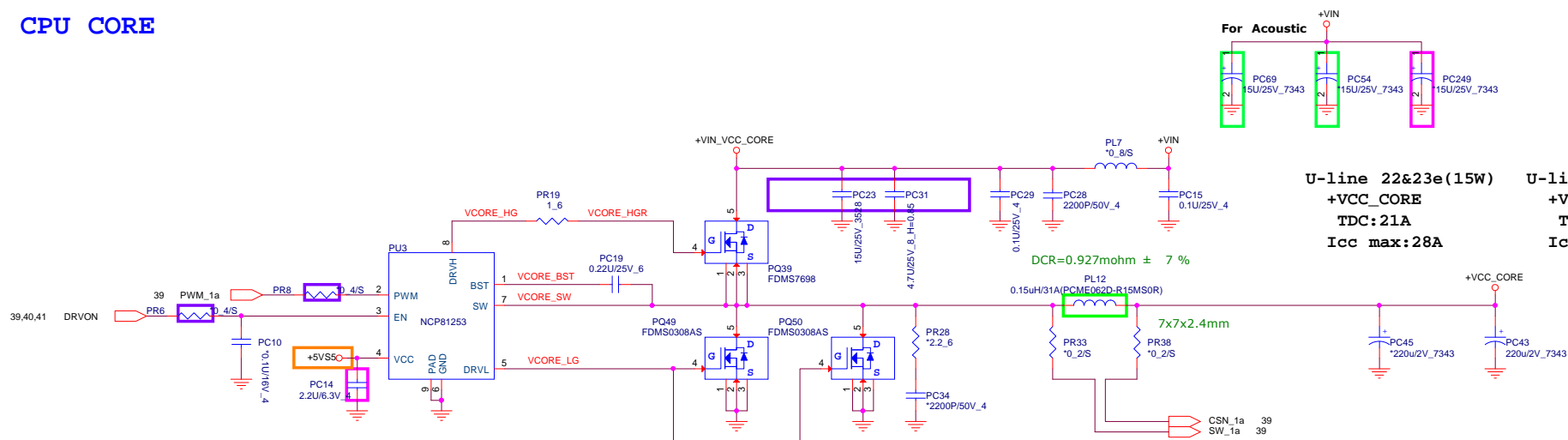




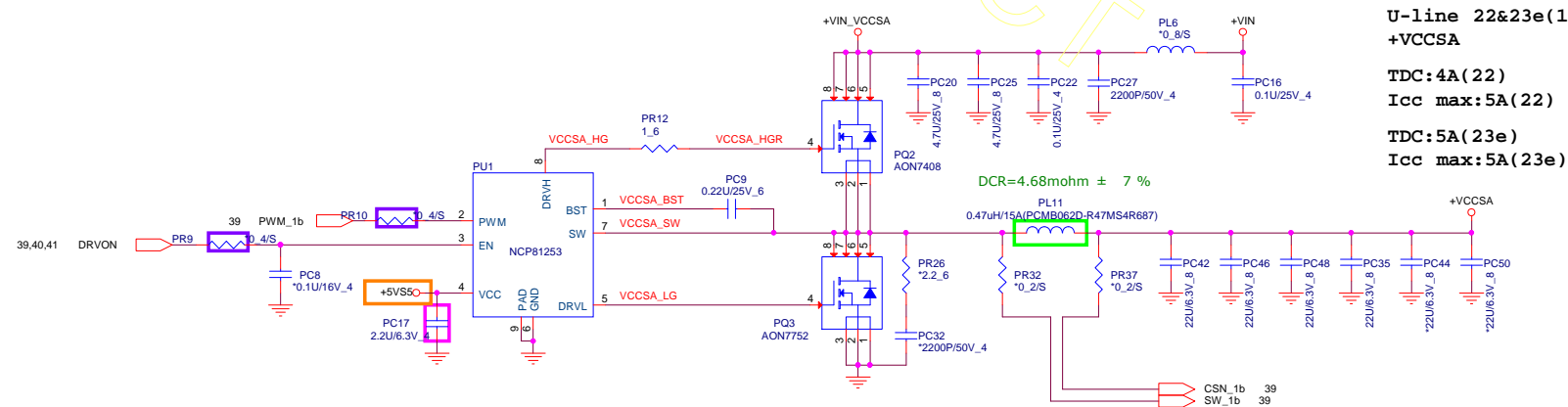




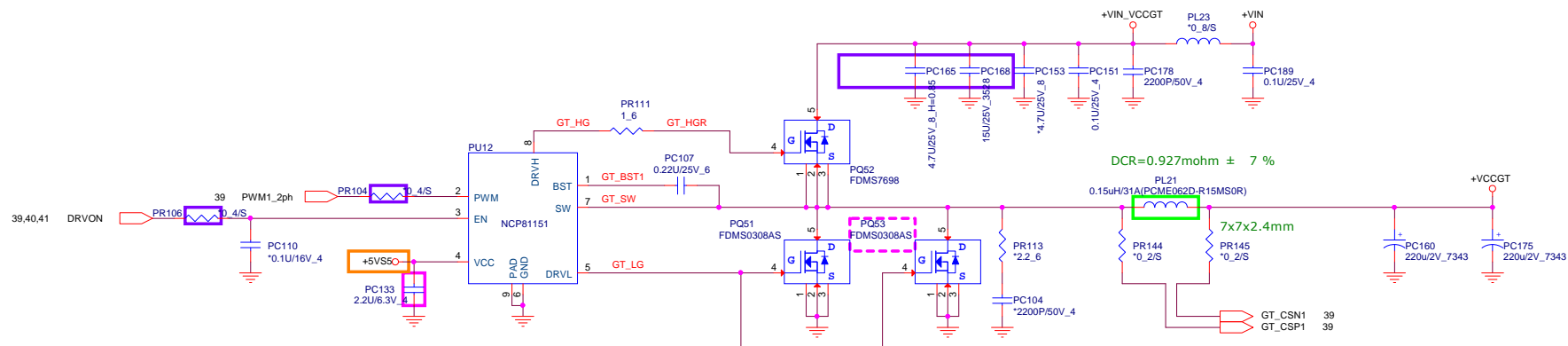
## CPU CORE



## VCCSA



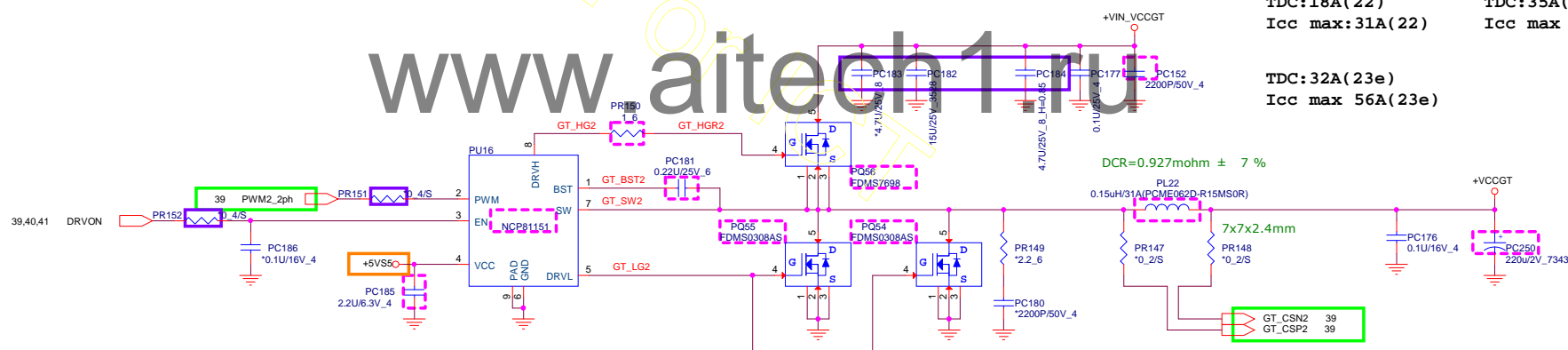
+VIN 20,28,31,33,34,35,36,39,40,42  
 +VCCGT 7,39  
 +VIN\_VCC\_CORE  
 +5VSS 4,22,25,26,34,35,36,37,38,39,40  
 +5V 22,23,24,28,38

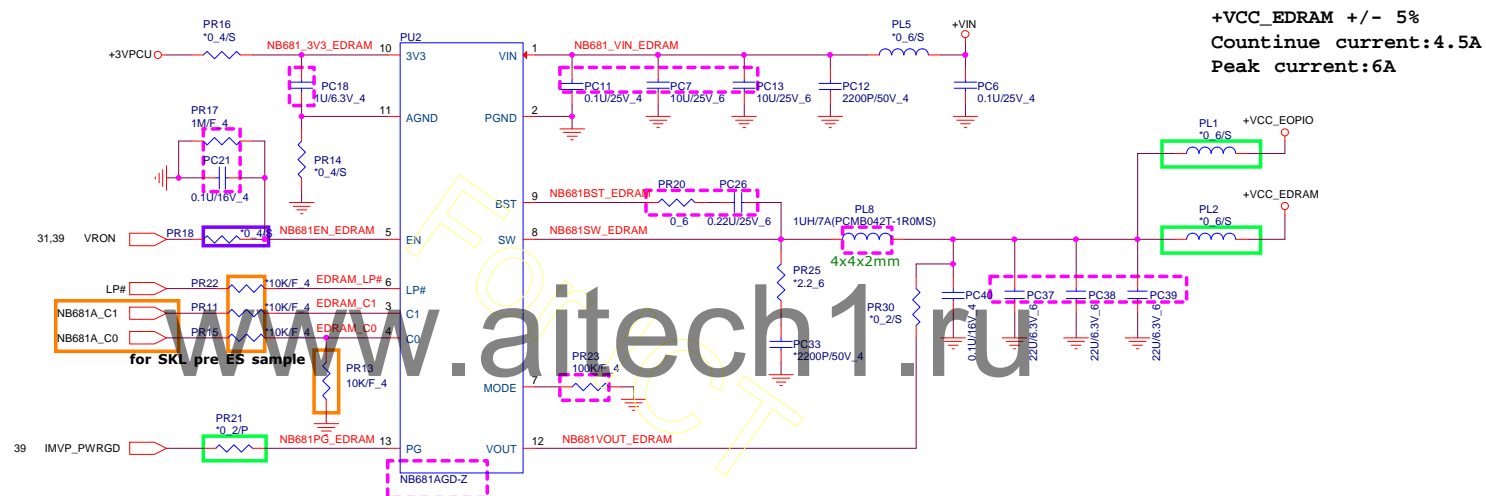
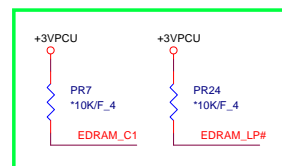


U-line 22&23e(15W) U-line 22&23e(28W)  
 +VCC\_GT +VCC\_GT

TDC:18A(22) TDC:35A(23e)  
 Icc max:31A(22) Icc max =57/7A(GTx)

TDC:32A(23e)  
 Icc max 56A(23e)





VCC\_EDRAM

LP#	C1	C0	Vout
0	X	X	0
1	0	0	0.8
1	0	1	0.95
1	1	0	1.0
1	1	1	1.05

MODE

	VR rail	Resistor
M1	VCCIO	0
M2	PRIMCORE	Float
M3	EDRAM/EOPIO	100K
M4	other	150K